Failures Analysis of Microcircuits

Titu-Marius I. BĂJENESCU[1]

[1] Prof., Doctor Honoris Causa of Military Technical Academy of Romania and of Technical University of Republic of Moldova (Chișinău); Romanian Academy Prize „*Tudor Tănăsescu*” Laureat

Abstract

For failure analysis of integrated circuits it is necessary to open and delayer a chip layer by layer in order to find a hidden defect or defects. It is necessary to determine the cause of failure to prevent future occurrence, and/or to improve the performance of the device. Increased circuit densities, smaller feature sizes and ever increasing multilayer technologies have created many challenges for failure analysis engineers.

Keywords: Microcircuits, reliability, failure, failure analysis, failure mode, failure mechanism

Received: 25 March 2019

To cite this article:
BĂJENESCU I. T.-M., “Failures Analysis of Microcircuits”, in *Electrotehnica, Electronica, Automatica (EEA)*, 2019, vol. 67, no. 2, pp. 84-88, ISSN 1582-5175.

Instead of introduction

In industry, in general, Failure Analysis (FA) is the scientific method of finding the cause of a product defecting that is, not performing — in its operation — the function for which it was created. Initially, FA was developed as an ancillary method of reliability research, being used to identify fault mechanisms for samples subjected to lifetime tests. Once the failure causes have been clarified for each defective test product that is, once the fault mechanisms have been established, some corrective measures (design changes, manufacturing process, input or flow controls, etc.) were proposed, which were applied to the following manufacturing batches for the same product. This procedure had a fundamental hurdle: it was used on the finished product, and the reaction was long delayed by the duration of the reliability tests (up to one year) and the subsequent analysis. So the corrective actions could not be applied to the next batch, but much later. Meanwhile a series of batches were manufactured with the same technology, which could be incorrect as a result of FA. That is why, in the last years FA has begun to be used throughout the development of a product [1].

Failure analyses are useful in all product development phases, from design to use [3]. At each of these stages, the results of the analyses will allow optimization of the products, ensuring their high reliability. Getting useful information at each stage of fault analysis is crucial, providing analyses with a high probability of success. For this, the laboratories are equipped with a full range of effective devices that allow for non-destructive testing, sample preparation, electrical, physical, and chemical characteristics of fallen components [4]. The success of the analyses is related to a rigorous methodology that requires the realization of a sequence of precise steps during the analysis. For starters, electrical failure characterization and non-destructive checks; followed by the step of preparing the sample that physically modifies the component and facilitates the identification of the defect. Another stage of preparation of the sample concerns access to the defective area and is often necessary to physically and chemically characterize the defect in the localized area [5-6]. From now on, the mechanism that has led to the failure can be understood. The chaining of these different steps must be done without loss of the defect and without giving rise to new defects that could cause the detection of the initial defect.

Case of microelectronic technologies

In the continued development of microelectronic technologies**, FA** allows — through the study of potential failure mechanisms — to define corrective solutions. For the implementation of localization and defect detection techniques, a key step is to prepare the samples. In order to adapt to the continuous progress of the field, by introducing new materials — which increase the complexity of the components — the preparation of the samples must evolve continuously [7-25].

Failure associated with wafer

To achieve a high-level of quality and reliability of microelectronic components since the 1960s FA laboratories have been extensively developed within the specialized industries. Their mission was to perform breakthrough performance analyses to understand their failure process, correct identified shortcomings, and improve long-term products to gain customer confidence.

In order to solve FA problems, two essential requirements must be met: *(i)* good theoretical and practical knowledge of the experimental techniques dedicated to the analysis; *(ii)* a rigorous working methodology to ensure the best possible choice in the various stages of fault analysis.

FA can also be defined as a diagnostic process whose purpose is to determine the cause of a malfunction. It has many applications in many industries, but it is particularly important in the integrated circuit industry (CI). These activities are used to determine the root cause of a malfunction to support the process of improving the yield, quality and reliability of the product. In a more limited use of the term, the failure analysis refers to the complete analysis of the semiconductor devices that have failed. This refers in particular to user returns, qualification errors and

technical assessments. In the broadest sense, fault analysis includes a wide range of diagnostic activities: include supporting the development process, eliminating design errors, and improving performance of the plate and its assembly work. Despite numerous diagnostic activities, a number of common tools and technologies have emerged that support the analysis of integrated circuit failures. For this reason, CI failure analysis offers an excellent perspective to address a discussion about these tools and technologies.

A comprehensive failure analysis procedure is given in Figure 1, and the flow analysis for failures is given in Figure 2.

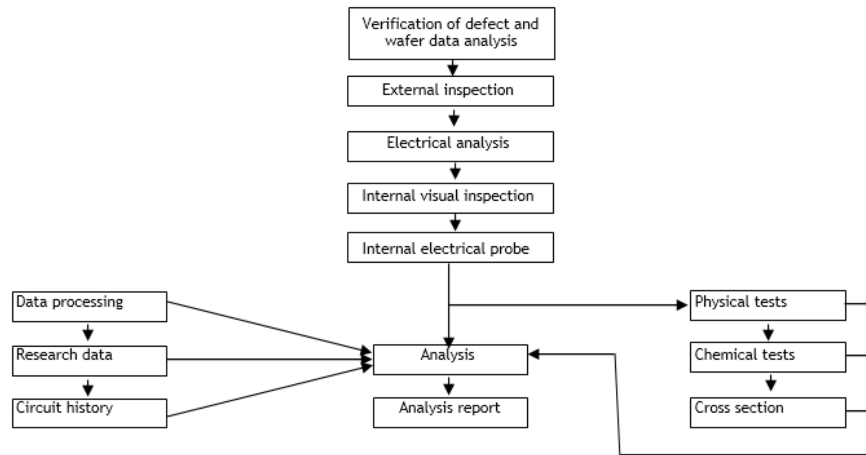

Figure 1. Procedure for failure analysis

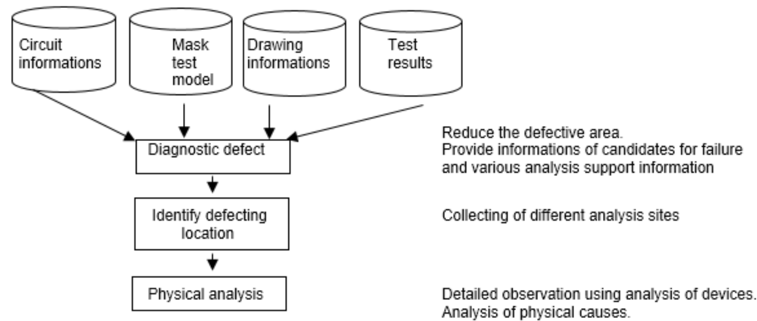

Figure 2. Flow for defect analysis

The tools and techniques used can be grouped into several sub-processes that form the flow of a generic failure analysis process.

Figure 3 shows a much simplified graphical diagram of the two flows of the fault analysis process.

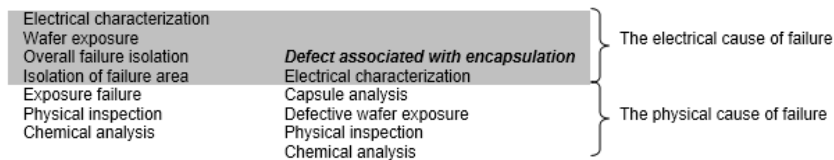

Figure 3. For comparison, the two flows of the failure analysis process are presented. Each flow can be broken down into an electrical cause and a physical cause of the failure

In fact, in a complete analysis of the failure, there are countless branches and decisions that are parts of the full process description. Generally, the process can be seen as being made up of two parts: *(i)* electrical isolation of the fault and *(ii)* analysis of the physical cause of the fault — as can be seen from Figure 3.

Electrical isolation can be seen as a restriction of purpose investigation, causing a more accurate electrical cause of the fault. For example, a precise electrical cause of the fault may be the short-circuit between two networks or between signal interconnections. The second part of the process is the determination of the physical cause of the fault: the process of discovering the physical cause that led to the electrical failure. If we go back to the example above, the physical cause of the failure may be a stainless steel particle that shorts the two interconnections.

As outlined above, the failure analysis process is in fact part of a larger process to improve the manufacturing or product. What drive us to analyse the failure is the fallen devices. In some cases, very specific — such as qualification failures — must be thoroughly and successfully analysed. In other cases, for example, performance analysis — where all

devices that are fallen, cannot be analysed, a selection process must first be done.

Usually the selection is made in such a way that the manufacturing process can be improved as much as possible. Typically, it consists of a Pareto ranking of the observed defect characteristics. The purpose of the failover analysis process is to enable an improvement process. Therefore, the result of the fault analysis — identifying the physical cause of the failure — should be useful for correcting the manufacturing problem. This leads to the need to identify the cause of the fault, which goes beyond the physical cause of the fault. The main cause of the particle cited in previous example may be the wrong design of the chip charger for the interconnect deposition device resulting in friction and particle generation.

In simple terms, the isolation process can be seen as a determination of focus attention to discover the defect or anomaly. The physical analysis process is one of exploring and collecting information about the failure mechanism or the physical cause of the failure. The process of corrective action consists in using the physical analysis to understand how the abnormality arose during the manufacture of the device and how the root cause of the failure can be eliminated.

Electrical characterization

Electrical characterization plays a very important role in defect analysis and is the first step in any analysis. The initial electrical verification process provides a general understanding of how the device is electrically defective. Generally, it is presented as a data log that measures the continuity, parametric and functional outputs of the device in the production test equipment. All this guides the continuation of action. The results may lead to the need for a more detailed characterization. For example, identifying a leakage can lead to a thorough characterization of the current-voltage characteristic (I-V) by means of a curve tracer or a parametric analyser. In the case of functional errors, their observation may result in a "Schmoo plotting" (characterization depending on temperature, voltage, or frequency of power supply); or can lead to a test scan to better understand the failure characteristics. This electrical characterization may later provide a partial or even complete identification of the defect. In highly structured devices — such as memories — this can lead to a conclusive identification of the failure location of a single bit of memory that occupies less than one micron square. When test design features — such as SCAN — are present in logic, they can often be used to isolate single node or network node failures. The initial electrical characterization may therefore provide us with indications of an encapsulation problem. In such cases, the non-destructive analysis of the capsule may occur prior to any subsequent activity.

So electrical testing is required to isolate the site of failure. Since fault isolation techniques are extremely diverse, they have two common requirements: They require the defective device to be placed in the fault condition and the characterization allows us to understand how the faulty device should be put in the defect condition(s).

Solicitation of the wafer

The chip is necessarily exposed to mechanical and electrical stresses in order to be able to use subsequent insulation techniques, as the capsule materials are opaque. Normally, the ceramic capsules are mechanically opened, while the plastic capsules are subjected to a specific decapsulation process. A critical requirement for these processes is to maintain the electrical integrity of the device. It is essential that the device breaks down the same way as before the chip has been exposed to decapsulation techniques. In addition, the external pins and their connections must remain intact so they can be used at a convenient polarization so that the fault area can be located. Because in most cases the surface of the chip is exposed, some technologies cannot expose the active face while maintaining the electrical functionality. An alternative is to expose and polish the back of the chip / plate using insulation loop techniques. Another alternative would be to completely remove the chip from the capsule. This leads to the removal of the usual electrical stimulation paths that are required to isolate the defective area. This can be remedied by re-encapsulation (placing the device in an alternative capsule more fit for defect analysis and reconnection of connections) or using a test card.

Isolation of the fault area

For this purpose, a wide range of techniques can be used to narrow the focus of the investigation diagnosis. Modern ICs have millions — if not billions — of transistors and interconnections. It is, therefore, impossible to analyse an IC without restricting the focus of the investigation diagnosis from millions to just a few transistors. Generally, techniques can be categorized into global techniques and testing techniques. Thermal detection techniques attempt to identify the heat generated by the site of failure. Likewise, photon emission microscopy identifies abnormal light emission as a result of an electron-hole recombination. A number of other techniques that identify different carrier beams or thermal events are effective methods for isolating the defective area.

Testing techniques are those that allow us to make electrical signal measurements within an IC. These techniques can be seen as device debugging techniques by direct measurement of circuit performance. If these techniques are applied without isolation of the area against electrical tests, the isolation process by testing can prove long and fastidious.

Analysis of encapsulation

The encapsulation analysis uses non-destructive techniques to analyse the structure of an IC. Electrical data may indicate a possible problem due to encapsulation — such as open, short-circuits or leakages. In such cases, it is useful to assess the physical condition of the capsule and its interior before any destructive analysis. These techniques therefore initiate the physical analysis of the cause of open circuit or short-circuit failures. Strong tests — such as X-ray and *Scanning Acoustic Microscopy* (SAM) — provide particularly useful information about the integrity of the capsule structure.

Physical and chemical analysis

The task of physical and chemical analysis is to support the determination of the physical cause of the failure. As soon as the failure site has been completely isolated, the analysis should be continued to identify the root / physical cause of the failure. Generally, three types of tools are used: sample preparation, physical observation and chemical analysis. Sample preparation techniques are used to remove materials that prevent access to the defective area. It's about manufacturing, polishing and cross-section.

Physical observation uses different types of microscopes: optical, scanning microscopes, electron microscopes, and more. Chemical analysis is used on defects to determine the root cause of the failure.

Diagnostic activities

For several decades, in many cases, the previously described diagnostic process was the standard procedure for defect analysis. The remarkable advances made by the semiconductor industry — in terms of continuous improvement of low-priced technology — have been successfully implemented. Many of the industrial trends that have led to this process have had a major impact on failure analysis (increased complexity of devices, smaller sizes, multiple interconnection levels, lower supply voltages and the evolution of surface mount encapsulations), and — in the end — chip scale packaging. These changes have resulted in the equipment needed to perform these much more sophisticated and costly failover analysis sub-processes. These changes led to the development of very different techniques and procedures. This is explained by the fact that many of the procedures give very good results for a class of failures, but are ineffective for other failures. For example, some faulty zone isolation techniques can be very well applied in order to open circuits, but do not provide benefits for leakage-related failures. Sometimes specific development tools have arisen due to a specific change that has occurred in industry. The use of double-layer metallization is largely responsible for the development of global fault isolation tools such as liquid crystals and photon emission microscopy. Similarly, surface mount technology has led to the development of SAM to detect and understand delamination observed during customer assembling of devices using surface mount technology. When the requirements for diagnostic activity have grown to become specialized, many tools have specialized for specific applications. For example, in-line instruments — such as SEMs and optical microscopes — have automated plate-handling capabilities and are compatible with the clean room to perform platelet performance analysis in manufacturing. Likewise, SAM applications have been adapted to allow 100% inspection of the devices after the assembly operation to ensure the adhesion of chip-encapsulating materials.

Just as the toolkit has expanded, the application of the fault analysis methodology has also expanded, becoming customized for a set of diagnostic activities. From a historical point of view, these tasks have been consolidated in the fault analysis laboratories. However, as the importance of different diagnostic activities was understood and the tools were personalized, activities became separate functions.

These sub-processes are used in full or in part in various diagnostic applications: process development, platelet performance analysis, design errors, assembling performance analysis, and customer return analysis.

The applications of different fault analysis techniques can be represented in an array in which diagnostic activities are compared with the instrument used in the failure analysis (Table 1).

Table 1. Diagnostic activities are compared either the instrument used to analyse the failures

Diagnostic activities		A	B	C	D	E
Process development *wafer* production yield analysis	Particle analysis		●			●
	Parametric analysis		●			●
	Performance analysis		●		●	●
Design errors			●		●	
Assembly performance analysis		●	●			●
Qualification	Return customer	●	●	●	●	●
Return customer	Qualification / reliability	●	●	●	●	●

Legend:

A — Capsule analysis
B — Electrical characterization
C — Chip exposure
D — Isolation of the failure site
E — Physical / chemical analysis

The electrical characterization (**B**) is a key element of all diagnostic activities.

Conclusions

The times in the life of a product, and also the ways in which FA must be present have been presented. These are: product development, manufacturing and use. In each case, the main features and role of FA were detailed. The industrial use of FA should become frequent for other areas of activity.

References

[1] Bâzu M. and T. Băjenescu (2011), Failure Analysis. A Practical Guide for Manufacturers of Electronic Components and Systems, J. Wiley & Sons.
[2] Băjenescu T. and M. Bâzu, (2010) Component Reliability for Electronic Systems, Artech House.
[3] De Wolf, I., (2006) Reliability issues in MEMS: Physics of failure and design for reliability, Patent DfMM & Memunity Workshop, 27 Nov. Milan, Italy.
[4] O'Connor, P. D. T.,(2000) Reliability past, present and future, IEEE Trans. on Reliability, Vol. 49, Issue 4.
[5] Greathouse, S. W., (2006)Application-specific reliability in new product applications, Future Fab Intl., Vol. 20, Intel Corporation, July.
[6] [6] Ion, R., (2005) Statistical model for estimating the failure probability in the field, Proc. of Ann. Reliab. and Maintainab. Symp. RAMS 2005, 256-260.
[7] Jensen, F., (2000) Electronic Component Reliability, Chichester, John Wiley & Sons.
[8] Johnson, S.C. (2009) Tessera working WLP, wafer-level optics. Semiconductor International, April 1, 2009.
[9] Gao, G. et al. (2008) Low-cost Compliant Wafer-level Packaging Technology, Tessera Internal Report, 2008, http://www.tessera.com/ technologies. (Accessed 2017).
[10] Pathangey, B. et al. (2007) Application of TOFSIMS for contamination issues in the assembly world. IEEE Trans. Device Mater. Reliab., **7** (1), pp. 11–18.
[11] Hoontrakul, P. et al. (2003) Understanding the strength of epoxy–polyimide interfaces for flip-chip packages. IEEE Trans. Device Mater. Rel., **3** (4), pp. 159–166.
[12] Suhir, E., Lee, Y.C. and Wong, C.P. (2007) Micro- and Opto-Electronic Materials and Structure: Physics, Mechanics, Design, Reliability, Packaging, Springer, New York.
[13] Bamal, M. et al. (2006) Performance comparison of interconnect technology and architecture options for deep submicron technology nodes. Proc. of Internat. Interconnect Technology Conference, pp. 202–204.
[14] Heng, E. (2010) Nano-wafer-level packaging to revolutionise semiconductors. Innov. – Mag. Res. Technol., **9** (1), www.innovationmagazine.com/ innovation /volumes /v3n4/free /features2.shtml.
[15] Stevens, C. Relay Failures Induced by the Growth of Tin Whiskers. A Case Study. http://nepp.nasa.gov/ WHISKER/reference/tech_papers/stevens2001-relay-

failures-induced-by-tin-whiskers.pdf. (Accessed 2017).
[16] Savi, J. (2001) Reliability of electronic assemblies. 38th Annual Spring Reliability Symposium: Reliability and Safety, May, 2001.
[17] LeBret, J.B. and Norton, M.G. (2003) Tin whiskers – a recurring industrial problem examined with electron microscopy. Microsc. Microanal., **9** (Suppl. 2), pp. 806–807.
[18] Odegard, C. and Lambert, C. (2000) Reflectometry techniques aid IC failure analysis. Test Meas. World, **1,** www.gigaprobestek.com/images/TDR_tecniques_aid_IC_FA_byTexas_Instruments.pdf.
[19] Ancona, M.G., Saks, N.S. and McCarthy, D. (1998) Lateral distribution of hot carrier-induced interface traps in MOSFETs. IEEE Electron Device Lett., **35** (12), pp. 2221-2228.
[20] Aichinger, T. and Nelhiebel, M. (2008) Advanced energetic and lateral sensitive charge pumping profiling methods for MOSFET device characterisation – analytical discussion and case studies. IEEE Trans. Device Mater. Reliab., **8** (3), pp. 509–518.
[21] Jaeger, R.C. et al. (1968) Record of the 1968 Region III IEEE Convention, pp. 58–191.
[22] Roedel, R. and Viswanathan, C.R. (1975) Reduction of popcorn noise in integrated circuits. IEEE Trans. Electron Devices, **ED-22**, pp. 962–964.
[23] Yamamoto, S. et al. (1971) On perfect Crystal Device Technology for Reducing Flicker Noise in Bipolar Transistors, Colloques Internat. CNRS No. 204, pp. 87–89.
[24] Zayats, A. and Richards, D. (2009) Nano-Optics and Near-Field Optical Microscopy, Artech House, Norwood, MA.
[25] Wagner, C. L. (Ed.), Failure Analysis of Integrated Circuits, Springer, 1999.
[26] Băjenescu, T.-M., Zuverlässigkeit elektronischer Bauelemente, Wiley-VCH, Weinheim, 2018.

Authors' Biography

Titu I. BĂJENESCU was born in Câmpina (Romania) on April 2, 1933.
He received his engineering training at the Polytechnic Institute Bucharest.
He served for the first five years in the *Romanian Army Research Institute*, including tours on radio and telecom maintenance, and in the reliability, safety and maintainability office of the Ministry of Defence (main base ground facilities).
R&D *Experience*: design and manufacture of experimental equipment for Romanian Army Research Institute and for air defence system.
He joined *Brown Boveri* (today: *Asea Brown Boveri*) Baden (Switzerland) in 1969, as research and development engineer.
R&D *Experience*: design and manufacture of new industrial equipment for telecommunications.
In 1974, he joined *Hasler Limited* (today: *Ascom*) Berne as Reliability Manager (recruitment by competitive examination).
Experience: Set up QRA and R&M teams. Developed policies, procedures and training. Managed QRA and R&M programmes. As QRA Manager monitoring and reporting on production quality and in-service reliability.
As Switzerland official, contributed to development of new ITU and IEC standards.
In 1981, he joined *Messtechnik und Optoelektronik* (Neuchâtel, Switzerland, and Haar, West Germany), a subsidiary of Messerschmitt-Bölkow-Blohm (MBB) Munich, as Quality and Reliability Manager (recruitment by competitive examination).
Experience: Product Assurance Manager of "intelligent cables". Managed applied research on reliability (electronic components, system analysis methods, test methods, etc.).
Since 1985, he has worked as an *independent consultant and international expert* on engineering management, telecommunications, reliability, quality and safety.
Mr. Băjenescu is the author of many technical books — published in English, French, German and Romanian.
He is emeritus university professor and has written many papers and contributions on modern telecommunications, and on quality and reliability engineering and management.
He lectures as invited professor, visiting lecturer or speaker at European universities and other venues on these subjects.
Since 1991, he won many Awards and Distinctions, presented by the Romanian Academy, Romanian Society for Quality, Romanian Engineers Association, etc. for his contribution to reliability science and technology.
Recently, he received the honorific titles of *Doctor Honoris Causa* from the *Romanian Military Academy* and from *Technical University of the Republic of Moldavia*.
In 2013, he obtained, together with prof. Marius Bâzu (head of reliability laboratory of Romanian Research Institute for Micro and Nano-technologies – IMT) the *Romanian Academy "Tudor Tănăsescu" prize* for the book *Failure Analysis*, published by John Wiley & Sons.
email-address: tmbajenesco@gmail.com