PACKAGING OF NANODEVICES AND RELIABILITY

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1. INTRODUCTION

Considered initially as an accessory, indented only to protect the die from the environment, the package has become more and more an essential part of the electronic component. First, because the increasing level of integration led to the more sophisticated packages, with multiple dies in the same package and using modern manufacturing materials. But also because for the newest type of device, the microsystem, the package has not only to protect the die from the environment, but also to ensure the interaction between the die (containing a sensor) and the environment. The package has an essential role in the operation of electronic components, based on three main functions: *(1)* To interface the die with the external circuit. *(2)* To remove the heat generated by device operation. *(3)* To protect the die from the external environment (mechanical integrity, protection from temperature, radiation, moisture, ions and so on, chemical isolation from harsh environment). The package must find the best compromise between electrical, thermal and mechanical performances and physical dimensions to meet product-specific applications, reliability and cost objectives.

The predictable future trends are towards nano-packaging for nanosystems. The first nano-packaging proposed as collaboration between Georgia Institute of Technology NUS and Institute of Microelectronics (IME) of Singapore promises to bring nano-interconnections at wafer level. A team of about 40 faculty, researchers and graduate students are exploring ways to develop nano-structured connections in the short term to 20 to 100 micrometer pitch and nano-grain or nano-fiber connections in the long-term to 1-micrometer pitch.

An ambitious research program of the Packaging Research Center of Georgia Institute of Technology has four main directions [1]: *(a)* Electrical design: design for wafer-level packaging, design of chip-to-package rigid/compliant lead transitions, power distribution with minimum noise and electro-migration, signal integrity; *(b)* Interconnects: lead-free solder, nano links, nano interconnections, micro-electromechanical systems (MEMS)-fabricated interconnects; *(c)* Test and burn-in: interposer with built-in test-support processor and large bandwidth capability, mixed signal test at ultra-high optical signal rate; *(d)* Reliability: micro scale and nano-scale material characterization, fatigue modeling and design for reliability (DfR).

When multiple dies are put in one package, this is called *system in package* (SiP). When multiple dies are combined on a small substrate, often ceramic, this is called *multichip module* (MCM) [2].

In recent years, a new category of packaging technology has begun to be used: *wafer-level package* (WLP). An example is *chip-scale package* (CSP), which entered the industry's lexicon in 1994 [3], and is defined as a package with a perimeter that is no more than 1.2 times the perimeter of the die it contains. Such packages combine the best features of bare die assembly and traditional semiconductor packaging, and reduce overall system size, something that is to be desired in portable electronic products. WLP is used for the technologies of packaging an IC at wafer level, instead of the traditional process of assembling the package of each individual unit after wafer.

2. NANOTECHNOLOGY AND SOME ASPECTS OF THE WLP RELIABILITY

Nanotechnology is the creation of functional materials, devices, and systems through control of matter on the nanometer (1 to 100 nm) length scale and the exploitation of novel properties and phenomena developed at that scale.

The semiconductor industry faces serious problems with power density, interconnect scaling, defects and variability, performance and density overkill, design complexity, and memory-bandwidth limitations. Instead of raw clock speed, parallelism must now fuel further performance improvements, while few persuasive parallel applications yet exist. A candidate to replace complementary CMOS, nanoelectronics could address some of these challenges, but it also introduces new problems (figure 1).

There are two major factors limiting the reliability of WLP, especially for die sizes larger than 5×5 mm: *(i)* interconnect fatigue due to stresses generated by the coefficient of thermal expansion (CTE) mismatch between the die and the PCB and *(ii)* packaging cost. For WLPs that require a redistribution layer (RDL) for I/O redistribution and a compliant layer for reliability, the electroplating process and the dielectric layer make up a large portion of the overall packaging cost. The costs of RDL for a WLP with two metal layers are even greater. Recently, *Tessera* has developed a new compliant WLP that dramatically lowers cost versus previous compliant WLPs [4]. The compliant layer is more cost-effective than spin-on polyimide, benzocyclobutene (BCB) - employed as a filling material for encapsulation - or silicone dielectrics, which are used in conventional WLPs. The copper conductor is etched (which is cheaper than electroplating) to form traces and protected with solder mask. Wirebonds are used to connect the individual die pads to the copper traces, and eventually encapsulation and solder ball attach complete the packaging process.

Under filling (UF) is used to solve reliability problems, because UF reduces the effect of CTE mismatch between the silicon chip and the substrate. Also, UF protects the chip against impurities and makes the structure mechanically stronger by minimising the stress levels or fatigue in the solder joints. However, the adhesion of the die side passivation (polyimide) to UF is critical to the reliability of flip chip (FC) assemblies [5]. Weak interfaces between the die polyimide layer and the UF resin can result in yield loss during thermal cycling or when exposed to a highly accelerated stress test environment of heat and humidity. UF materials absorb moisture, and accumulation of moisture at the interfaces can lead to: *(a)* Crack propagation caused by swelling stress. *(b)* Weakening mechanical support. *(c)* Die-level interconnect failures. *(d)* Corrosion due to ionic contaminants resulting in metal migration failures.

3. 3D PACKAGE

A 3D package contains two or more chips stacked vertically so that they occupy less space. The concept was developed for IC, but could be applied to other electronic components. The names used are system-in-package (SiP) or chip stack multi-chip module (MCM). The wiring of the stacked chips is done along their edges, increasing the length and width of the package and usually requiring a supplementary layer between the chips. The solution to avoiding such an increase of package dimensions is to use through-silicon vias (TSVs) to wire the chips. TSVs are vertical connections through the body of the chips. Consequently, a TSV 3D package (also called TSS – through-silicon stacking) can also be flatter than an edge-wired 3D package, but is smaller in length and width. TSV technology has a wide range of applications: cell phones, MP3 players, notebooks and digital still cameras. Being a new technology, the reliability issues of TSVs are not yet completely understood.

3D interconnects offer an attractive option to reduce the energy dissipation and propagation delay of long on-chip wires (51 and 54% reduction in latency and energy dissipation respectively at 45 nm node). Also, optical interconnects offer reduced latency compared to scaled Cu/low-k technologies, but do not offer significant improvement compared to other technologies like WLP interconnects. A good solution might be the carbon nanotube (CNT) interconnects, which are compared favourably with scaled Cu/low-κ interconnects in terms of latency, with a 42% reduction in delay [6].

Heat-transfer analysis and thermal management of nanodevices become more complex when packing different functional components into a tight space. The miniaturization also raises issues such as coupling between system configurations and the overall heat dissipation to the environment.

4. PROCESS ERRORS

The main possible process errors are: *(i)* Faults in the seal glass (cracks, voids or migration), leading to leakage – intermittent or open circuit – to be identified by stress tests (seal, electrical, high-temperature-storage, temperature cycling and high-voltage tests). *(ii)* Incomplete hermetic seal (for metallic or ceramic packages), producing characteristic degradation or short circuit due to chemical corrosion or humidity. A seal test is needed to identify the failure risks. *(iii)* Dielectric particles floating in the package that may produce intermittent or short circuit. The recommended stress sequence for eliminating these failures is: constant acceleration, vibration (monitored), radiography, and shock (monitored) test. *(iv)* Broken or bent external lead, which leads to open circuit and can be identified by visual inspection followed by lead-fatigue test.

5. PLASTIC PACKAGE

The material used for plastic encapsulation is thermo-reactive resin: a combination of phenol and epoxy resins or silicone resins. The moulding material contains a basic resin, a drying agent, a catalyst, an inert material, an agent for firing delay and a material facilitating the detachment of the package after the moulding operation. If chosen properly, the moulding material may diminish the action of various failure mechanisms produced at wafer level, such as intermetallic Au bond–Al pad interface, which may lead to corrosion and failure at operation above 180°C. It is necessary to choose the right moulding compound alternatives, such as environmentally friendly halogen-free compounds, to mitigate high temperature corrosion. A study focused on this subject offered a characterization of bromine-related wirebond weakening processes, establishing the high-temperature reliability of halogen-free moulding compounds [7].

An ideal moulding compound has: low permeability to moisture, high strength at elevated temperatures, a high glass transition temperature and excellent adhesion. Much research on moulding compounds has been directed towards reducing their moisture permeability and raising their temperature gradient, in order to increase their high temperature strength. Newer biphenyl resins have been developed with filler content approaching 90%, considerably reducing the moisture permeability of the moulding compound. Though the strength of the moulding compound also decreases, the compensation derived from the reduction of moisture absorption counterbalances this at reflow temperatures.

It is important to determine the appropriate size of the spherical silica filler particles included in the package body to ensure thermal cycling-related reliability in plastic-encapsulated packages [8]. This is because the thermal shrinkage of the plastic package body can cause serious damage to the active pattern of the device due to the compressive stress resulting from the fillers pinned by the lead frame. In particular, the model suggested in this work indicates that the combined action of a large filler and smaller fillers can become a failure-causing factor in the plastic package. Thus the adoption of an appropriate filler size in the plastic encapsulation might allow a greater reliability margin for the modification of the lead-on-chip package structure.

In a plastic-encapsulated leaded surface-mount package, the failure mechanism known as *creep corrosion* will only be a reliability concern if the corrosion product is electrically conductive and bridges across two electrical paths, such as leads. The failure mode is generally current leakage [9].

When plastic encapsulated microcircuits (PEMs) underwent a few hundred hours in a steam pressure pot (SPP) test, a harsh moist environment, high leakage currents were noticed. Two possible causes were identified: *(i)* mould compound and *(ii)* the polyimide tape used for co-planarity of lead-frame fingers [10]. It seems however that the leakage current is independent of the frame and is not caused by the mould compound, but rather by the ionic content and acrylic-based adhesive layer of the polyimide tape. Ionic leakage current may occur as a result of moisture penetrating the package and accumulating at the chip. Moisture can reach the chip via penetration along the plastic–lead frame interface, through pores and cracks, as well as via vapour diffusion through the electromagnetic compatibility (EMC). Polyimides, like epoxies, can absorb several weight per cent of moisture, affecting both their mechanical and their electrical properties. The solution proposed for eliminating the high leakage current is to use polyimide tape with low ionic content and non-acrylic-based adhesive.

Failures in plastic packages caused by thermo-mechanical stress may occur at die or plastic level. The lead frame can initiate failure in the die or plastic, leading to an increase in the thermal resistance of the package. Die-related failures include: metal shift, die cracking, electrical failure, filler particle point failure and passivation damage. Plastic-related failures are concerned with the formation of cracks in the body of the package. Plastic cracks are usually derived from the delamination of the plastic from the plastic–silicon interface or the plastic–die paddle interface, which can give rise to the popcorn cracking [10].

The combination of moisture absorbed in the plastic and thermal stresses caused by the different expansions of the metal lead frame and the plastic may produce cracks in larger plastic surface mounting packages, initiated by internal stresses during soldering. Some results show that a critical amount of moisture absorption may lead to cracking, which can be diminished by baking procedures [11].

The primary cause of corrosion, stiction or other failure mechanisms within hermetically sealed enclosures has historically been viewed as due to increases in internal moisture concentrations. It has historically been postulated that the primary source of moisture in these enclosures is the failure to achieve at seal, or the loss of hermeticity post-seal.

Empirical observation of many data sets over the past 20+ years shows that this postulation does not always hold up in practice. The purpose of the current work is to test this postulation through the analysis of archival microelectronic packages and data sets of various ages [18].

6. ASPECTS OF MEMS/NEMS PACKAGING

As nanotechnology and MEMS are enabling new discoveries in diverse fields of science and engineering [12], a collection of review papers have been seen recently that try to summarize the various impacts that nanotechnology is bringing. Focusing on different physical and statistical issues, these review papers have provided a general background of reliability research in nano-engineering.

Motivated by a recent prediction made by Semiconductor Industry Association (SIA) in the International Technology Roadmap for Semiconductors (ITRS) [13] that the silicon technology will continue its historical rate of advancement with the Moore's law for a least of couple of decades, the paper [14] indicates that the silicon gate oxide will be scaled down to its physical limit. An alternative way is to replace oxide with a physically thicker high-k material to help solve most of the problems. However, new problems concerning reliability and performance have to be addressed. The paper [15] reviewed the status of reliability studies of high-k gate dielectrics and illustrated some concepts with experimental results.

Packaging is one of the key issues to be addressed for the evaluation of the reliability of MEMS/NEMS (nano-electro-mechanical switches) products. Any defects created during the sealing of packaging process may cause immediate device failure or may degrade the device performance over time. Furthermore, thermal stress induced by CTE mismatch is one of the main factors that affect the packaging reliability. In fact, the formation of the stress can happen not only during packaging process but also during the operation of devices. Such temperature variations cause the expansion of packaging materials when they are constrained by the package assembly. As a result of this mismatch, significant stresses are induced in the package and may cause the device to fail.

In addition to thermal mismatch, corrosion, creep, fracture, fatigue crack initiation and propagation, and delamination of thin films are all possible factors that may cause the failure of packaged devices. These failure mechanisms could be present or deferred by using proper packaging designs.

The strain can be further reduced if excellent thermal paths are built around interconnects to alleviate thermal stress originating from the temperature gradient between the ambient and operation temperature. On the other hand, delamination phenomena occur in the interface of adjacent material layers such as components made of dissimilar materials that are subsequently bonded together. Delamination can result in electrical or mechanical failures of devices such as mechanically cracking through the electrical via wall to make an electrical open because of the propagation of the delamination of metal line from the dielectric layer or overheating of the die because of delamination of the underside of the die, causing openings in the heath dissipation path. That is why the development of the packaging designs to increase the reliability is very important and requires extensive investigations.

Reliability testing is required before a new device can be delivered to the market. The test results can provide information for the improvement of packaging design and fabrication. The analyse method is to use the mathematical tools of probability and statistical distribution to evaluate data to understand the patterns of failure and to identify the sources of failure [16].

7. CONCEPTS AND TERMINOLOGY

A clear understanding of several concepts and terminology related to reliability is needed to proceed with the understanding of the methodologies which are applied to guarantee optimal operability of VLSI and ULSI systems, fault tolerance, and circuit architectures implementing them. IEEE defines reliability of a system or component to perform its required functions under stated conditions and for a specified period of time. The process yield of a manufacturing process is defined as the fraction, or percentage, of acceptable parts among all parts that are fabricated. A system failure occurs or is present when the service provided by the system differs from the specified service or the service that should have been offered.

Nano-reliability measures the ability of a nano-scaled product to perform its intended functionality. At the nano-scale, the physical, chemical, and biological properties of materials differ in fundamental, valuable ways from the properties of

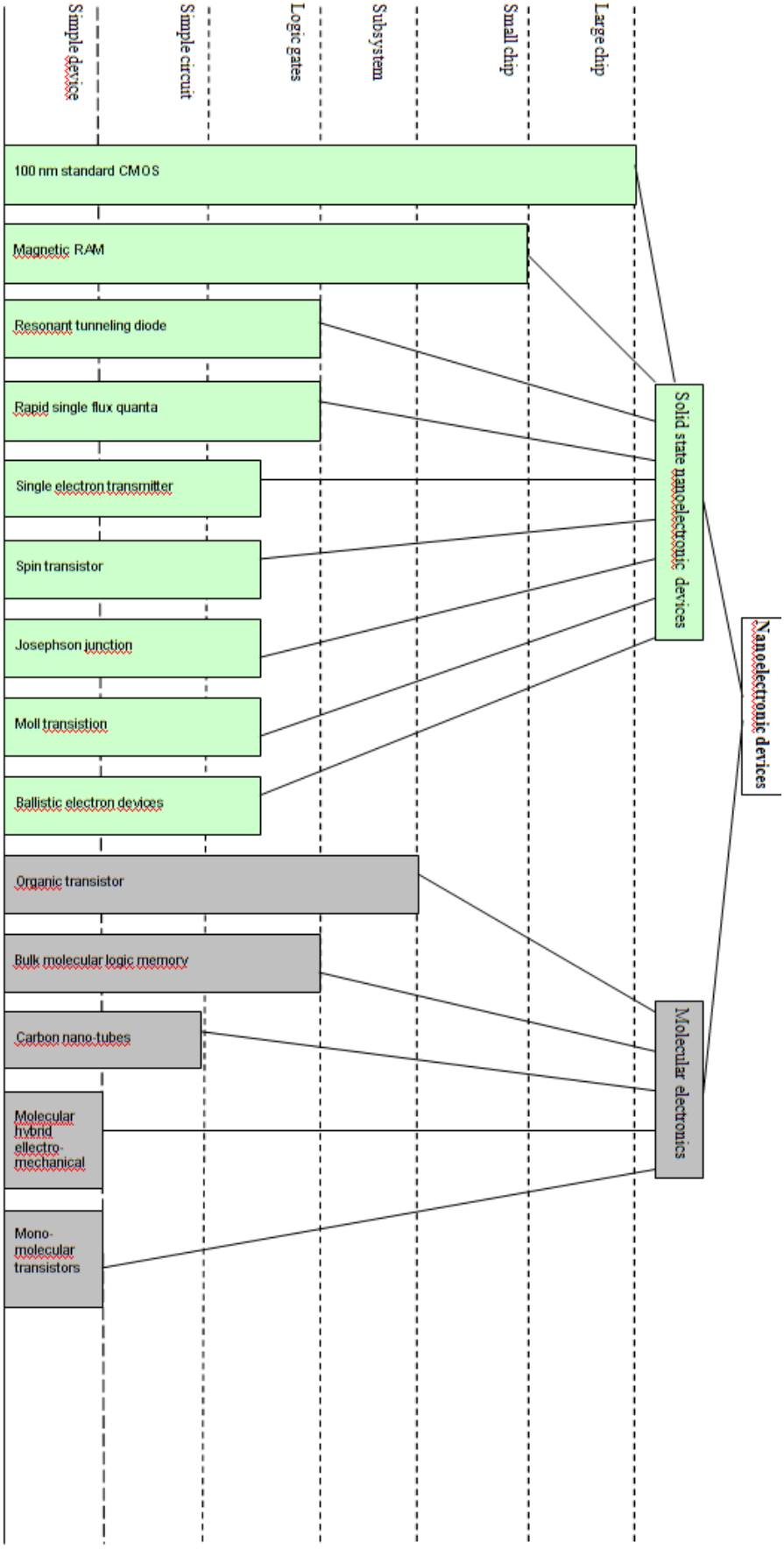
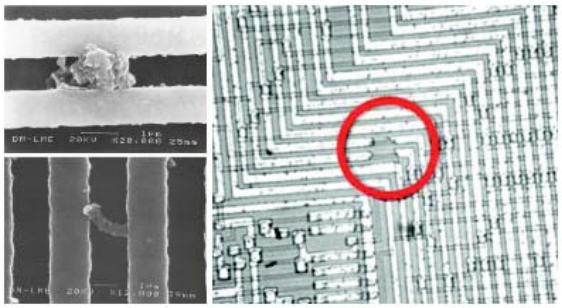


Figure 1. The roadmap for nanotechnology presents many nanodevices currently being investigated as an alternative to standard CMOS [13].

individual atoms, molecules, or bulk matter.

Conventional reliability theories need to be restudied to be applied to nano-engineering. Research on nano-reliability is extremely important due to the fact that nano-structure components account for a high proportion of costs, and serve critical roles in newly designed products.

The ability to measure, and manipulate matter at the atomic/molecular scale has led to the discovery of novel materials. A nanometre is 10^{-12} metre, a single human hair is about 8×10^5 nanometres wide.



a. *b.*

Figure 2. Defect images: **(a)** Bridging defects with low-resistance electrical behaviour on the top and high-resistance electrical behaviour on the bottom microphotograph, and **(b)** Open defect inside the circle [17]

The upper layer of a fault model models various physical defects such as missing spot, unwanted spot, gate oxide short (GOS) with channel, floating gate coupled to a conductor, and bridging faults. Some of the physical defects are depicted in figure 2. The fault models have been developed from structural and lithography defects, and each defect model is described in terms of electrical parameters of its components. Thus, for simulation purposes, physical defects are translated into equivalent electrical linear devices such as resistors, capacitors and nonlinear devices such as diodes and scaled transistors [17].

CMOS technology on silicon is the dominating technology for microelectronic systems. Figure 3 shows a technology landscape until the year 2015 to give an overview about the whole area of potential technologies for information processing. Apart from solid-state nanoelectronics other technologies such as opto-electronics, super-conductive and molecular electronics are depicted.

A wrong output signal produced by a defective system is called an error. An error is an effect whose cause is some defect. Errors can be

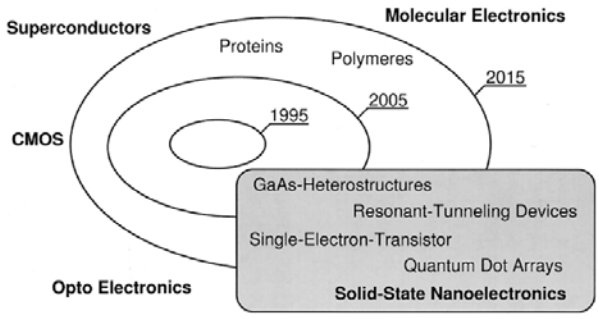


Figure 3. Landscape of different technologies for future information processing [19].

classified into three main groups: permanent, intermittent, and transient errors (the last ones are temporal single malfunctions caused by some temporary environmental conditions which can be an external phenomenon such as radiation or noise originating from other parts of the chip) [20].

8. CONCLUSIONS

The correct solution for modeling MEMS devices is to use physical models: full-finite element simulations of the naked die or packaged device. This is a time-consuming task, so the companies are reluctant in using such approach. Very often, independent research groups are involved in such activities. An example is the research group from the Polytechnic University of Milan led by Prof. Alberto Corigliano, which has developed a useful model for the effect of various mechanical and environmental factors on MEMS reliability [21, 22].

References

1. *Packaging Research Center, Georgia Institute of Technology, http:///www.nsf.gov/pubs/2000/nsf00137q.html*

2. Bâzu, M., Băjenescu T. *Failure Analysis. A Practical Guide for Manufacturers of Electronic Components and Systems, Wiley, Chichester and New York, 2011.*

3. Thomson P. *Chip Scale Packaging, IEEE Spectrum,* Vol. 36, pp. 36-43.

4. Gao G. et al. *Low-cost Compliant Waferlevel Packaging Technology. Tessera Internal Report,* 2008, http://www.tessera.com/ technologies

5. Pathangey B. et al. *Application of TOFSIMS for Contamination Issues in the Assembly World. IEEE Trans. Device Mater. Reliability, Vol. 7, No. 1, pp. 11-18.*

6. Bamal L. et al. *Performance Comparison of Interconnect Technology and Architecture Options for Deep Submicron Technology Nodes. Proc. of Internat. Interconnect Technology Conf., 2006, pp. 202-204.*

7. Chandrasekaran A. *Effect of Encapsulant on High-temperature of the Gold Wirebond-Aluminum Bondpad Interface, Master of Science Thesis, University of Maryland, 2003.*

8. Lee S. M. *Filler-induced Failure Mechanism in Plastic Encapsulated Microelectronic Package. Metals Mater. Int., Vol. 12, No. 6, pp.513-516.*

9. Xie J., Pecht M. *Palladium-plated Packages; Creep Corrosion and its Impact on Reliability," Advanced Packaging, February 2001.*

10. Kelly G. *The Simulation of Thermomechanically Induced Stress in Plastic Encapsulated IC Packages, Kluwer, Dordrecht, 1999.*

11. Lea C., Tilbrook D. *Moisture Induced Failure in Plastic Surface Mount Packages," Soldering Surf. Mount Technol., Vol. 1, No. 3, pp. 30-34.*

12. Huff M. *About MEMS and Nano-technology. http://www.memsnet.org/mems/*

13. *ITRS, "International Technology Roadmap for Semiconductors," http://www.itrs.net/reports.html*

14. Wong H., Iwai H. *On the Scaling Issues and High-Kappa Replacement of Ultra-Thin Gate Dielectrics for Nanoscale MOS Transistors. Microelectronic Engineering, Vol. 83, pp. 1867-1904.*

15. Ribes, G. et al. *Review of High-k Dielectrics Reliability Issues. IEEE Trans. Devices and Materials Reliab., Vol. 5, pp. 5-19.*

16. Bhushan, B. *Nanotechnology, 2nd edition, Springer, Berlin and New York, 2007.*

17. Stanislavjević M. et al. *Reliability of Nanoscale Circuits and Systems. Methodologies and Circuits Architecture, Springer, Berlin and New York, 2011.*

18. Lowry R. K., Kullberg R. C. *Examining internal gas compositions of a variety of microcircuit package types and ages with a focus on sources of internal moisture. Paper # 7206-1 presented during MF102 7206 Reliability, Packaging, Testing, and Characterization of MEMS/MOEMS and Nanodevices VIII, 28 Jan 2009 to 29 Jan 2009.*

19. Goser F. K. et al. *Aspects of Systems and Circuits for Nanoelectronics. Proc. of the IEEE, Vol.85, No. 4, pp. 558-573.*

20. Jeng Sh.-L. et al. *A review of Reliability Research on Nanotechnology. IEEE Trans. on Reliability, Vol. 56 (2007), No. 3, pp. 401-410.*

21. Mariani S., Ghisi A., Corigliano A., Zerbini S. *Multi-Scale Analysis of MEMS Sensors Subject to Drop Impacts. Sensors, Vol. 7, 2007, pp. 1817-1833.*

22. Mariani S., Ghisi A., Corigliano A., Zerbini S. *Modeling Impact-Induced Failure of Polysilicon MEMS, a Multi-Scale Approach. Sensors, Vol. 9, 2009, pp. 556-567.*

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