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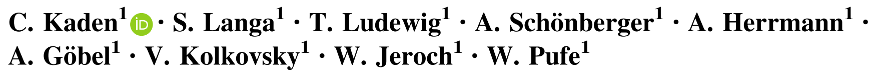
TECHNICAL PAPER

Enhancement of vertical integration density by engineered BSOI wafers



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Abstract The lateral and vertical integration density of bulk microelectromechanical systems (MEMS) using bonded silicon-on-insulator (BSOI) wafers is significantly enhanced if the handle wafer is used as an electrical redistribution layer. Therefore isolated conductive paths should be integrated in the handle wafer, which are connected to the surface of the BSOI-wafer by high aspect ratio contacts (VIAs) through the device layer of the BSOI-wafer. In the present study we report on a fabrication process for customer specific designed BSOI wafers with VIAs from the device to the handle layers. Wafer bonding, wafer edge shaping and thinning of the wafers, which are critical processes for the fabrication of the BSOI-wafers, are discussed. The contacts to the handle wafer through the 75 µm thick device layer are created by 10 µm wide and 75 µm deep trenches filled with highly doped *n*-type polysilicon. From current–voltage measurements an ohmic behaviour of the contacts with a resistance of around 120 Ω is demonstrated.

1 Introduction

System in Package (SiP, Tai 2000) is an effective approach to gain more functionality of devices by integrating several MEMS devices and their controlling units into one functional package. SiP can be implemented as lateral integration (2D), lateral and vertical (2.5D) or pure vertical integration (3D). However, due to the die-level integration of the different components within SiP, the packaging costs can become very high. In this case System on Chip (SoC) (Benini and De Micheli 2002) can be used as an alternative approach. Similarly to SiP, SoC can be realized in three different configurations 2D, 2.5D or 3D. However the integration on wafer-level reduces the packaging costs significantly.

In the present paper an approach to enhance the vertical integration density of MEMS-devices fabricated on the basis of bonded silicon-on-insulator (BSOI) wafers is discussed. BSOI-wafers are widely used e.g. for the fabrication of MOEMS (Grahmann et al. 2015; Langa et al. 2013), pressure sensors (Li et al. 2015; Ngo et al. 2015), inertial sensors (Abdolvand et al. 2007) and energy harvesters (Nimo et al. 2011).

In the past there have been approaches to engineer the BSOI handle or device wafer before bonding, see e.g. PBSOI (patterned BSOI) for vertical transistors (Moriceau et al. 2004; Kim et al. 2005).

A typical BSOI wafer (Fig. 1) consists of three main components: a handle wafer (e.g. 400–700 µm thick), a device wafer (e.g. 5–200 µm thick) and a buried oxide layer (BOX, e.g. 0.1–1 µm thick). The handle and the device wafers are bonded together by fusion bonding, the BOX is used as bonding and isolation interface between the wafers. The MEMS devices are usually structured in the device layer of the BSOI wafer and the handle wafer is only used for mechanical stability purposes.

Our approach is to define conducting paths in the handle wafer before bonding and connect them by VIAs in the device layer to the surface of the BSOI-wafer. In this case the handle wafer can act as an electrical redistribution layer and can replace conducting layers originally placed on the surface of the BSOI wafer. Since the conducting paths are processed before wafer bonding, the applied materials must

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