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TECHNICAL PAPER

Wafer level vacuum packaging of micro-mirrors with buried signal lines

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Abstract This paper presents the vacuum wafer level packaging of in-house manufactured two-dimensional micro- mirrors based on the electrostatic driving principle, fabricated using a bulk technology on bonded-silicon-on-insulator wafers. The so called buried signal line concept is used in order to obtain a wafer bond friendly bonding frame. Two versions of the buried signal line concept are described in the paper: crystalline Si and poly-Si based. Anodic and glass frit bonding methods were used to bond a stack of four wafers, resulting in a vacuum-sealed package. The fabrication technology, alignment, bonding, dicing and electrical characterization are discussed. A vacuum level of 120 Pa with no getter materials was reached in the package. Due to vacuum packaging the driving voltage of the micro-mirrors after dicing could be significantly decreased from approximately 170 V to less than 35 V.

1 Introduction

Many challenges have to be addressed during a vacuum wafer level packaging (VWLP) process of MEMS devices (Hofmann et al. 2008; Tachibana et al. 2009; Riley 2004; Baert et al. 2004; Gooch and Schimert 2003; Marinis et al. 2007). Some of these challenges are the concept, design and fabrication technology of the so called bonding frames (BF), i.e. the areas where the top and bottom wafers come into contact during the bonding procedure. The main parameters of a bonding frame designed for vacuum packaging are the width and the topography/roughness. The width of the bonding frame can be easily changed in the design process without a significant change in the technological process flow. A possible disadvantage of increasing the width of the bonding frame is certainly the impact on the chip size. In contrast, the topography improvement of the bonding frame, e.g., peak-to-peak roughness, often requires major changes in the technological process flow and this could bring additional costs. Therefore, simple solutions for decreasing the topography of the BF, which do not require significant changes in the standard process flow, are desired.

For MEMS technologies which do not have through silicon via (TSV), one of the major contributor to the topography of BF are the signal lines, i.e., the metal wiring, which are connecting electrically the device inside the package and the contact pads outside the package. The peak-to-peak topography generated by the signal lines is determined by the thickness of the used metal layer and is in the range of several hundreds of nanometers. This means that the bonding method (Tong and Goessele 1998; Dragoi 2009) used for the vacuum packaging should fulfill two major conditions (a) be robust enough in order to level out these high peak-to-peak values and (b) simultaneously should be "gentle" enough not to damage the signal lines during the bonding procedure.

For example, the glass frit bonding method (Knechtel 2005) can fulfill the first condition. However, taking into account that the signal lines are usually made of Al or AlSiCu, the high bonding temperature (more than 400 °C) and the high chuck pressure applied during the bonding procedure could damage the signal lines. Thus, this bonding method exposes a serious concern about fulfilling the second condition mentioned above. In order to address these issues during the vacuum packaging of micro-mirrors, two buried signal line concepts were developed and will discussed in this paper.

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