INVARIANT SAMPLE-AND-HOLD AMPLIFIER TO THE HOLD CAPACITOR DISCHARGE

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Abstract

The conventional measurement signal sample-and-hold amplifier comprising a sample and hold circuit in the form of a sample switch, a voltage hold capacitor, and a voltage repeater further includes two similar sample-and-hold circuits of reference voltages. The idea of the proposed amplifier is that hold capacitors are equally discharged in all three sample-and-hold circuits. Therefore, an affine ratio for the stored three voltage samples does not change the intrinsic value over a long discharge time. Then, this invariant affine ratio is taken as the measuring signal. A reproducing (recovery) unit, which is also included, calculates this affine ratio. In turn, the included information signal former shaper pre-converts (prepares) the initial measurement signal using reference voltages. Thus, the hold time is significantly increased, while maintaining a short sample time for the given hold capacitor. On the other hand, the affine ratio uses differences and voltage ratios. Therefore, offset errors are mutually reduced. It is possible to implement the proposed sample-and-hold amplifier in the form of an analog chip based on a multiplier and the known multi-channel sample-and-hold amplifier.

Keywords: sample-and-hold, affine ratio invariant, offset errors, capacitor discharge

Rezumat

Dispozitivul de eșantionare și stocare a valorilor de tensiune instantanee, care conține primul bloc de eșantionare și stocare a tensiunii sub formă de comutator de eșantionare, un condensator de stocare a tensiunii și un repetor al acestei tensiuni, adițional mai conține două blocuri de eșantionare și stocare a valorilor tensiunilor de referință. Esența dispozitivului constă în aceea, că în toate cele trei blocuri de eșantionare și stocare, condensatorii de stocare se descărcă identic. Prin urmare raportul simplu pentru cele trei eșantioane de tensiuni stocate nu își modifică valoarea într-o perioadă îndelungată de descărcare. Totodată, raportul simplu, ca o

valoare invariantă, este luat ca semnal de măsurare. Blocul de recuperare a semnalului de măsurare realizează calcularea acestui raport simplu. La rândul său, este inclus un semnal de informare care transformă (pregătește) semnalul de măsurare inițial folosind tensiunile de referință. Astfel, timpul de stocare crește semnificativ la menținerea timpului de eșantionare pentru condensatorul de stocare predeterminat. Pe de altă parte, raportul simplu folosește diferențele valorilor de tensiune. Prin urmare, erorile de compensare se reduc reciproc. Este posibilă realizarea dispozitivului propus sub forma unei microscheme analoge în baza unui multiplicator și unui dispozitiv multicanal pentru eșantionare și stocare cunoscut.

Cuvinte cheie: eșantionare și stocare, raportul simplu invariant, erori de compensare, descărcarea condensatorului

1. Introduction

Sample-and-hold amplifier (SHA, or track-and-hold amplifier) is an important component of different data converters and digital systems, such as signal processing systems, multichannel data acquisition systems, automatic test equipment, medical and analytical instrumentation, event analysis, analog-to-digital converters (ADCs), digital-to-analog converters (DACs), etc. It captures an analog signal and holds it during some operation (most commonly ADC).

Regardless of the circuit details or type of SHA in question, all these devices have four major components [1]. The input buffer amplifier, energy storage device (hold capacitor C_H), output buffer amplifier, and switching circuit are common to all SHAs as shown in the typical configuration of Fig. 1.

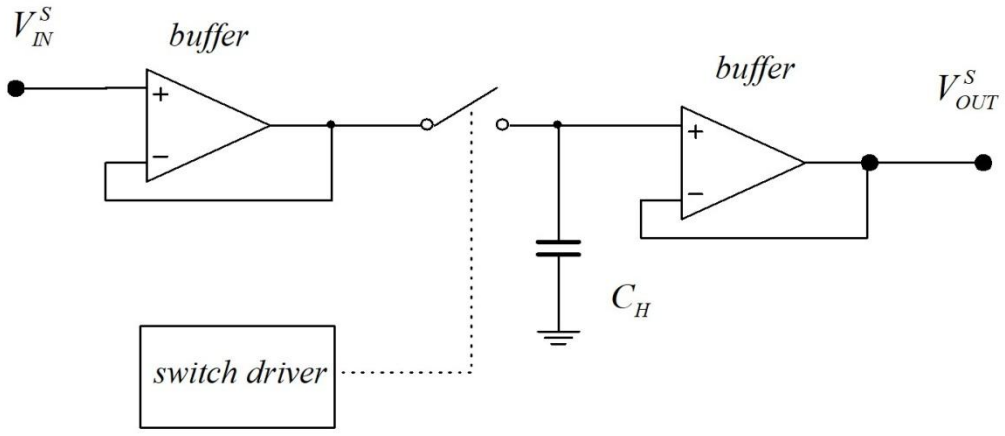


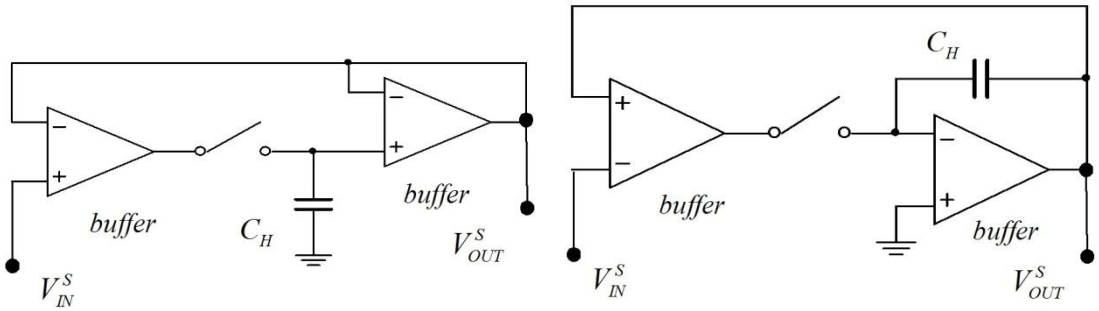
Fig. 1. Basic SHA.

The energy-storage device—the heart of the SHA—is a capacitor. The input amplifier buffers the input by presenting a high impedance to the signal source and providing a current gain to charge the hold capacitor. In the *track* mode, the voltage across the hold capacitor follows (or tracks) the input signal (with some delay and bandwidth limiting). In the *hold* mode, the switch is open, and the capacitor retains the voltage present before it was disconnected from

the input buffer. The output buffer offers a high impedance to the hold capacitor to keep the held voltage from discharging prematurely. The switching circuit and its driver form a mechanism by which the SHA is alternately switched between track and hold.

In the hold mode, there are errors due to imperfections in the hold capacitor, switch, and output amplifier. If a leakage current flows out of the hold capacitor, it will slowly discharge. This effect is known as *droop* in the SHA output. Droop can be caused by leakage across a dirty board if an external capacitor is used, or by a leaky capacitor; however, it is most commonly attributed to the leakage current in semiconductor switches and the bias current of the output buffer amplifier. Droop can be reduced by increasing the value of the hold capacitor; however, it will increase the acquisition time and reduce the bandwidth in the track mode.

There are direct current DC errors due to the summation of bias or offset voltages of the buffers. In versions of SHAs with a higher static accuracy, a common feedback loop can be used as in Fig. 2; at the same time, the sample speed decreases.



a) b)

Fig. 2. Sample-and-hold amplifiers with a common feedback loop:
(a) with a voltage repeater and (b) with an integrator.

Industry offers a wide range of SHA chips. In particular, the SMP04 device made according to Fig. 1 provides a high accuracy, a low droop rate, and a fast acquisition time required by date acquisition and signal processing systems [2]. A typical representative of closed SHA with the repeater is the LF398 chip [3]. An example of a SHA with an integrator is the SHC5320 device [4].

One way or another to be chosen, there is a contradictory problem of sampling performance and long hold time. The present paper proposes an alternative non-feedback SHA. The conventional measurement signal SHA comprising a sample-and-hold circuit (SHC) in the form of a sample switch, a voltage hold capacitor, and a voltage repeater further includes two similar SHCs of reference voltages. The idea of the proposed amplifier is that hold capacitors are equally discharged in all three SHCs. Therefore, an affine ratio for the stored three voltage samples does not change the intrinsic value over a long discharge time. Then, this invariant affine ratio is taken as the measuring signal. The included reproducing (recovery) unit calculates this affine ratio. In turn, the included information signal former pre-converts (prepares) the initial measurement signal using reference voltages. Thus, the hold time is significantly increased, while maintaining a short sample time for the given hold capacitor.

On the other hand, the affine ratio uses differences and voltage ratios. Therefore, offset errors are mutually reduced.

2. Proposed Non-Feedback SHA

The scheme in Fig. 3 includes a source of analog input measuring signal V_{IN}^{S}; the first maximum and second minimum sources of reference voltages V_2 and V_3; information signal former V_1; the first, second, and third SHCs; and analog output signal V_{OUT}^{S} reproducer.

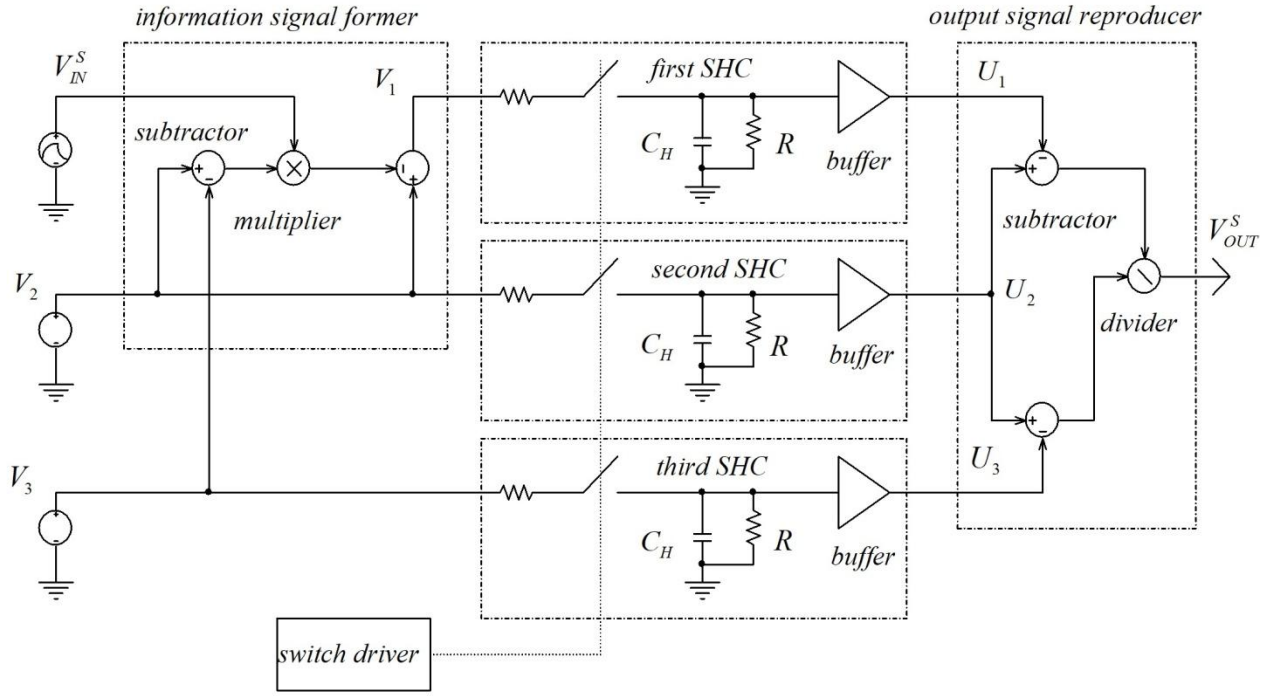


Fig. 3. Proposed SHA.

Each SHC has respectively a switch, hold capacitor C_H with an equivalent discharge resistor R, and a voltage repeater or buffer. The information signal former comprises a multiplier element and two subtractor elements. The output signal reproducer contains two subtractor elements and a divider element.

The SHA in Fig. 3 operates as follows. The measuring signal V_{IN}^{S} and reference voltages V_2, V_3 are supplied to the information signal former, which prepares the initial measurement signal. The obtained information signal V_1 is delivered to the first SHC. Similarly, the reference voltages are applied to the second and third SHCs.

In the *track* mode, the switches are closed, and the hold capacitors quickly charge. In the *hold* mode, the switches are open, the hold capacitors are equally discharged, the held information signal U_1 and reference voltages U_2, U_3 are supplied to the output signal reproducer. The output signal reproducer calculates the unvarying value V_{OUT}^{S} over a long discharge time.

It is known that the capacitors discharge is described by the following expressions:

$$U_1 = V_1 e^{-t/RC_H},\ U_2 = V_2 e^{-t/RC_H},\ U_3 = V_3 e^{-t/RC_H},$$

where V_1 is the information signal initial value and RC_H is the electric discharge time constant equal for the all hold capacitors.

The output signal reproducer calculates the following affine ratio [5, p. 131]:

$$V_{OUT}^S = \frac{U_2 - U_1}{U_2 - U_3} = \frac{V_2 e^{-t/RC} - V_1 e^{-t/RC}}{V_2 e^{-t/RC} - V_3 e^{-t/RC}} = \frac{V_2 - V_1}{V_2 - V_3} = V_{IN}^S.$$

It is evident that the affine ratio is independent of the discharge time and determined only by the initial voltage values. In addition, multiplicative and additive errors of U_1, U_2, U_3 values are mutually reduced. This formula determines the information signal:

$$V_1 = V_2 - V_{IN}^S (V_2 - V_3).$$

The information signal former operates according to this expression.

To increase the stability of the capacitors discharge, forced discharge resistors R can be directly introduced, in particular, to control the equal discharge. Therefore, there are no high requirements for limiting board leakage currents.

It is possible to use another affine ratio form to increase the change range, [5, p. 133]:

$$V_{OUT}^S = \frac{U_2 - U_1}{U_1 - U_3} = \frac{V_2 - V_1}{V_1 - V_3} = V_{IN}^S.$$

Then, the information signal is as follows:

$$V_1 = \frac{V_2 - V_{IN}^S V_3}{V_{IN}^S + 1}.$$

The corresponding information signal former will be constructed according to this expression; however, this case may be more difficult due to the use of a division element.

For both versions of the affine ratio, the reference voltage values are selected behind the information signal variation region, i.e., if

$$V_{1MIN} \le V_1 \le V_{1MAX}, \text{ then } V_2 > V_{1MAX},\quad V_3 < V_{1MIN}.$$

In practice, the output signal reproducer is directly implemented on an industrial chip, for example, an MPY634 multiplier in the two-voltage divider mode [6]. The information signal former is similarly executed. In addition, three SHCs are performed on an industrial device, for example, SMP04 [2]. Therefore, it is possible to accomplish the proposed SHA in the form of a united analog integrated circuit.

The paper describes only the theoretical idea of the SHA. It is only natural that modeling and experimental studies are required to determine the parameters of this device and the preferred application. It is reasonable to expect that the described version of the amplifier more suppresses offset errors than differential circuits, for example, on amplifiers with switched

capacitors [7, 8].

5. Conclusions

(i) There is a contradictory problem of sampling performance and long hold time for known SHAs.

(ii) There are direct current errors due to the summation of offset voltages of the buffer amplifiers without a common feedback loop.

(iii) The proposed SHA without feedback provides fast sample and long hold time.

(iv) For the used affine ratio, additive and multiplicative errors of voltage sample measurement are mutually reduced.

(v) It is possible to accomplish the proposed SHA in the form of a united analog integrated circuit using known devices and technology.

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References

[1] Sample-and-Hold Amplifiers, https://www.analog.com/media/en/training-seminars/tutorials/MT-090.pdf

[2] CMOS Quad Sample-and-Hold Amplifier SMP04, https://www.analog.com/media/en/technical-documentation/data-sheets/SMP04.pdf

[3] Sample-and-Hold Amplifier LF398, http://datasheet.su/datasheet/National%20Semiconductor/LF398

[4] High-Speed, Bipolar, Monolithic Sample-and-Hold Amplifier SHC5320, https://datasheet.su/datasheet/Burr%20Brown/SHC5320

[5] A. Penin, Analysis of Electrical Circuits with Variable Load Regime Parameters: Projective Geometry Method, 3rd ed., Springer International Publishing, Cham, Switzerland, 2020, p. 520.

[6] Wide Bandwidth Precision Analog Multiplier MPY634, http://datasheet.su/datasheet/Burr%20Brown/MPY634

[7] Ya. Chen, Yo. Chen, Y. Guo, and C. Li, Electronics 8 (9), 986 (2019).

[8] H. D. Rico-Aniles, J. Ramírez-Angulo, A. J. Lopez-Martin, R. G. Carvajal, J. M. Rocha-Pérez, and M. P. Garde, IEEE Access 8, 66508 (2020).