DESIGN AND EVALUATION OF A DIGITAL WIRELESS DEVELOPMENT PLATFORM

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ABSTRACT

As Wireless Personal Area Networks (WPAN) become more popular, new features and functionalities are added to these devices. Where, in the beginning, only data transfer was required, nowadays e.g. location awareness of WPAN devices is wanted[1][2].

WPAN protocols like Bluetooth and Zigbee can be implemented quite easily, but the available devices have a pre-established functionality. This fixed functionality is, when it comes to evaluating forthcoming WPAN features, an unwanted limitation. To evaluate these new functionalities a dynamic programmable wireless system is needed.

This paper describes a development platform for digital wireless systems in the 2.4 GHz ISM (Industrial Scientific Medical) frequency band. The first part of the paper deals with the hardware description of the platform and the discussion of its capabilities. In the second part a test set-up is described. Finally, the platform is evaluated.

Keywords: Wireless, Digital, development platform, 2.4GHz ISM band

INTRODUCTION

WPAN devices, like Bluetooth and Zigbee, are designed for wirelessly sending low rate data over a short range[3][5]. When thinking of adding new features to the existing functionality of WPAN devices it is necessary to have a general programmable environment which can transmit and receive signals in the frequency band of interest. In the case of Bluetooth and Zigbee, this is the 2.4GHz ISM frequency band[4][5]. WPAN devices provide low data rate, so it is not necessary to cover the 2.4 GHz ISM band as a whole. The system should be designed to select only a limited part of the ISM frequency band. However, it should be capable to dynamically select a limited band within the

2.4GHz to 2.483GHz range. (These are the Belgian frequency limits of the 2.4GHz ISM frequency band [6])

In the next paragraph a description of a hardware platform which meets both requirements of being general programmable and covering the whole frequency band is introduced.

HARDWARE DESCRIPTION

The general development platform consists of two main blocks as shown in Figure 1. The first block is an RF board based on a direct down converter (Maxim's max 2820). The second part is a board containing an FPGA (Xilinx Virtex II) and two fast ADC's (Analog Devices AD6644).

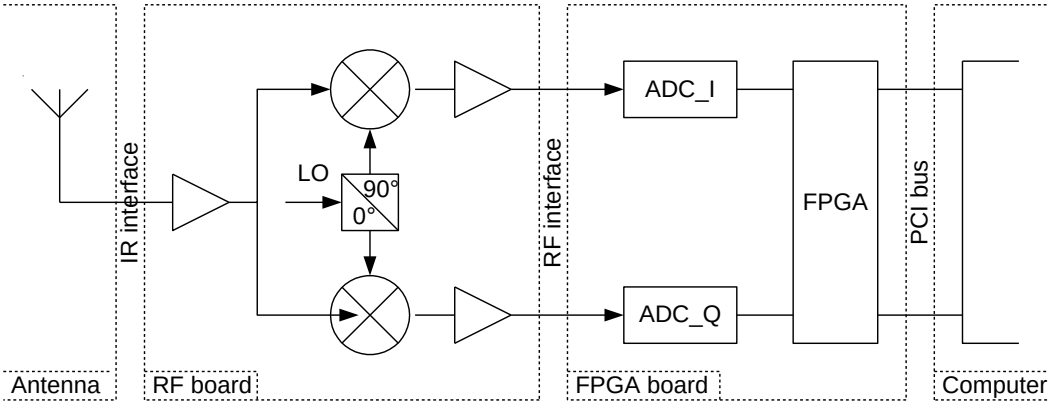

Figure 1: Block diagram of development platform

The incoming RF signal, at receiver site, is directly converted into a base band signal using the max 2820 down converter[7]. The normalized receiver response of the down converter is shown in Figure 2. It shows that the bandwidth of the system is 5MHz.

A reference clock input is used to generate the local oscillator (LO) signal. This reference clock can be either 22MHz or 44MHz. With this reference clock the max 2820 component is able to generate a LO signal of 2.4 to 2.5 GHz. Within this range, the LO frequency can be changed in steps of 1MHz [7].

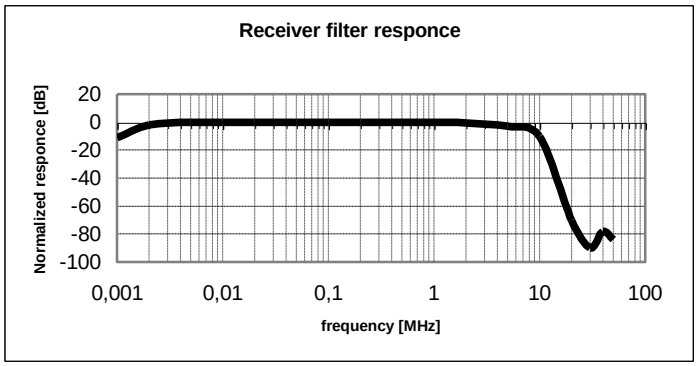

Figure 2: Normalized filter response max2820

After the down converter two 14 bit ADC's convert the analog signal into a digital one. This signal is then passed to the Virtex II FPGA. The FPGA can be programmed in a general way.

The FPGA board is equipped with a PCI compatible bus. When this board is mounted into a PCI slot of a PC it's possible to transfer data between the FPGA and the PC. This can be done both from and towards the computer. The PC can do further calculations on the received signals and bring the result to its output channels.

TEST SET-UP

To evaluate the platform a test set-up is made. In this set-up the developed platform is programmed as a receiver of a wireless communication system which uses a data rate of 500Kbps. The system uses a four differential phase shift keying (4DPSK) modulation scheme[8]. The carrier frequency is 2.45GHz. At the transmitter and receiver side a rooted raised cosine filter (RRC) with a roloff factor of 0.5 is used[9].

The packets which are sent out by the system consist of a symbol synchronisation, a bit synchronisation and a payload field (Figure 3). The symbol synchronisation field contains 3200 "1" bits. Hence the I-component of the modulated signal becomes a continuous sinus wave. The bit synchronisation part is 200 bits long. Here a fixed bit pattern is used. The payload part has a fixed length of 24000 bits and contains the actual data.

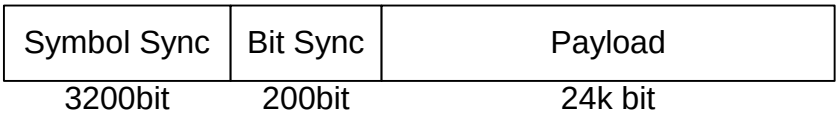

Figure 3: structure of the PHY packet

In what follows a description of the down conversion, synchronisation and demodulation scheme is given.

As mentioned above the LO frequency of the max 2820 down converter can be dynamically changed. By setting the frequency of the down converter to 2.45GHz the output of the max 2820 component is the base band modulated signal. The ADC's convert the analog base band modulated signal into a digital one. A sample frequency of 2MSps is used. This combined with a data rate of 500Kbps and a 4DPSK modulation means an over sample factor of eight is used (eight samples per symbol). Each sample is represented by an eight bit number.

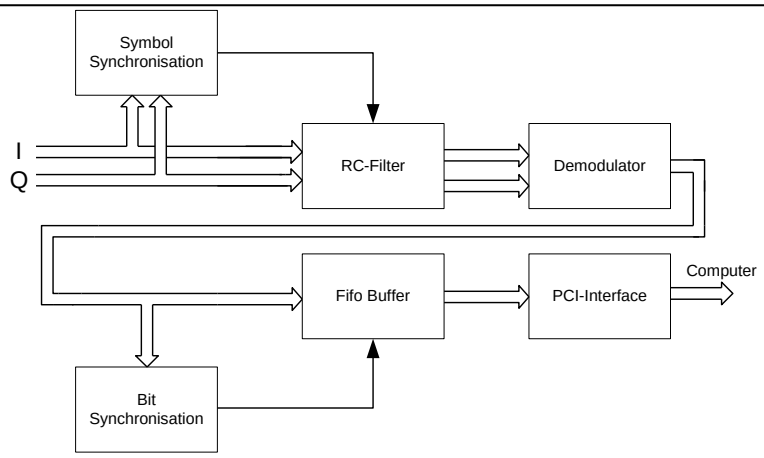

Figure 4: Blocks implemented in the FPGA

Synchronisation and demodulation of the signal is done by the FPGA. The diagram of the blocks implemented in the FPGA are shown in Figure 4. The demodulator is preceded by the Symbol synchronisation and RRC filter and followed by the bit synchronisation block, a FIFO buffer and the PCI interface logic.

Figure 5 shows the I and Q component of the base band modulated signal at the input of the FPGA. As described, the first field of the PHY packet is the symbol synchronisation part. This field can be seen on the left of both the I and Q component and distinguished from the bit synchronisation and payload part.

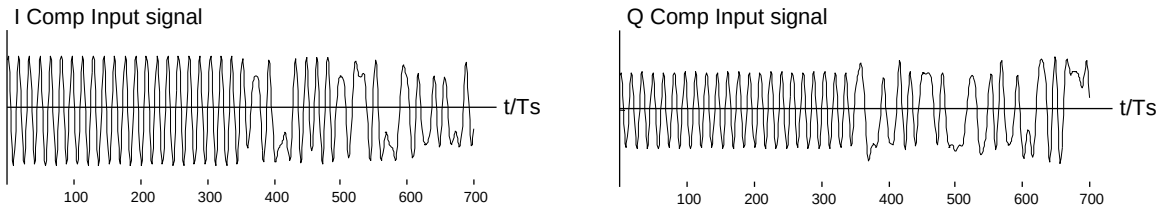

Figure 5: Input of the synchronisation block

In spite of the fact that the Q component of the symbol synchronisation part is zero at the transmitter, this is not the case at the receiver. The reason for this is that the receiver is not perfectly locked to the carrier frequency of the received signal. This leads to a rotation of the complex input signal when representing it into the complex plane. For the demodulation this is not a problem since DPSK modulation is used. For the synchronisation, on the other hand, this needs to be taken into account.

The symbol synchronisation block consists of three parts: the radius calculation, the correlation filter and the peak detector (Figure 6). The first block calculates the square of the radius of the incoming complex value. The output of this block is shown in Figure 7.

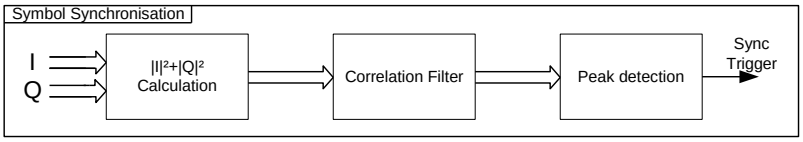

Figure 6: Block diagram Symbol synchronisation

Notice again the difference between the synchronisation part and the rest of the PHY packet. At this point, the synchronisation part has a maximum every eight samples. This because of the over sample value of the ADC and the shape of the synchronisation pulse. To further emphasize this periodic maximum a correlation filter is added to the system. Here the incoming signal of this filter is correlated with the value of the square of the synchronisation pulse used at transmitter side. The advantage of this filter is that the peaks of the synchronisation part are emphasized. The signal after the correlation filter is shown in Figure 8.

The last part of the synchronisation system is a peak detector. This peak detector searches for 255 successive maxima with a distance of eight sample values. If 255 successive maxima are found a sync trigger is generated. Now the demodulation process can start.

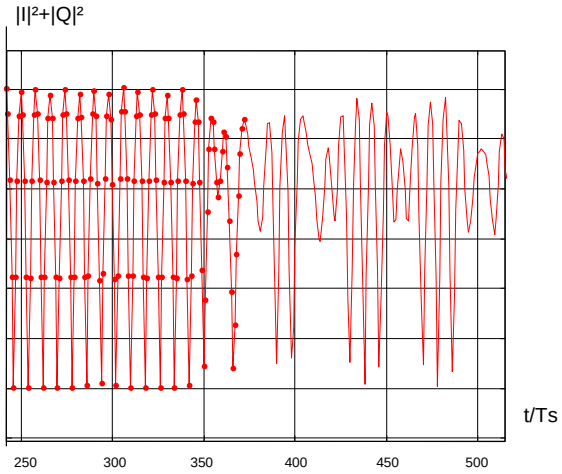

Figure 7: Input of the synchronisation filter

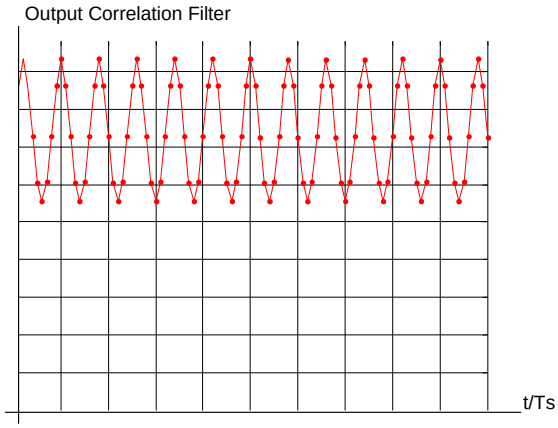

Figure 8: Input of the peak detector

Before the base band modulated signal at the input of the FPGA is demodulated it is filtered by a rooted raised cosine filter. In this implementation a filter with 31 taps and a roloff factor of 0.5 is used. After this filter the signal can be demodulated.

The demodulation algorithm used in the FPGA will be explained using Figure 9. Here the base band modulated signal is shown in the complex plane. The four points on the left plot are the constellation points which can be send out in 4DPSK modulator. At the demodulator the received constellation points are shown in the right plot of Figure 9.

To demodulate the signal it is necessary to know the angle between the current and the previous constellation point. In this case the angle is first estimated, afterwards it is used to do the actual demodulation. The estimation of the angle is done by subdividing the IQ plane in to 16 areas (as shown in Figure 9) and calculating how many areas lay between the current and previous constellation point. This angle gives, after consulting a look up table, the demodulated signal.

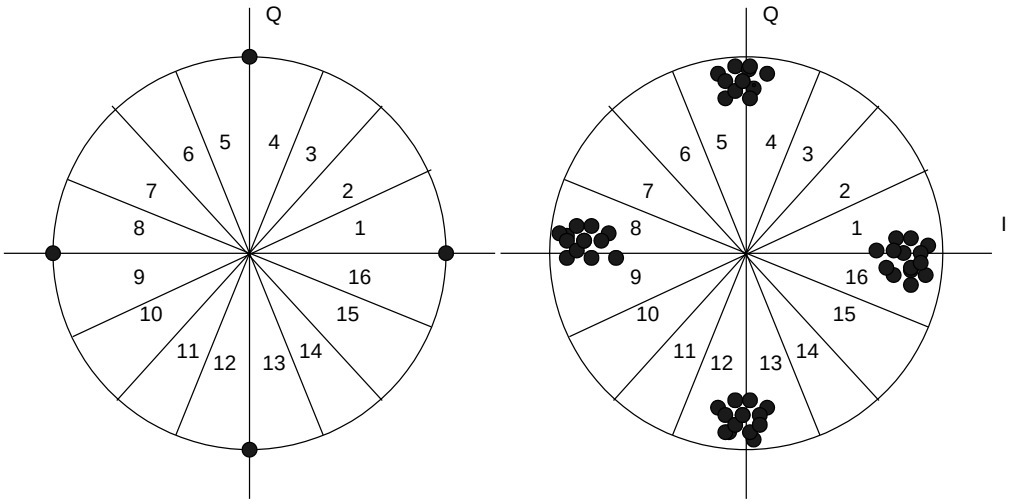

Figure 9: IQ plane constellation points at transmitter and receiver

After the demodulation, it is still necessary to detect the start of the payload part of the PHY packet (Figure 3). The bit synchronisation of the PHY packet is used for this purpose. By calculating the correlation between the demodulated signal and the transmitted bit synchronisation part of the PHY packet, the start of the payload is found. The payload data is pushed into a FIFO buffer. This buffer is emptied by a computer which gives, by using its PCI bus, pop commands. The received signal can now be further analysed on the computer.

CONCLUSIONS

In this paper, a general development platform for low rate communication systems in the 2.4GHz ISM frequency band is given. This system is build using the max 2820 down converter and a Xilinx Virtex II FPGA.

The max 2820 down converter is used to transform an incoming RF modulated signal into its base band representation. The FPGA can be programmed to do real time calculations on the base band modulated signal. The result of these calculations can be sent to a computer using a PCI interface. The system is able to dynamically cover the whole 2.4GHz ISM frequency band. The Receivers bandwidth is 5MHz. These specifications meet the goal to make a general development platform for low rate wireless systems in the 2.4GHz frequency band.

Further the implementation of a test set-up proves that the system works. In the test set-up 4DPSK modulated RF packet is down converted and demodulated by the platform. This demodulated signal is sent to the PCI slot of a computer where it can be further analysed.

In the future the system can be used to evaluate new algorithms and features for wireless low rate standards in the 2.4GHz frequency band.

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