DESIGN FOR TESTABILITY OF COMBINATIONAL CIRCUITS

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Abstract : A new concept of design for testability is being proposed, based on the properties of signals, gates and logical structures. This allows obtaining of reconfigurable elementary digital structures (REDS), which can work both in normal mode and in testing/ diagnosis mode. In the same way as on a filed covered with snow any non-uniform object can be observed, the digital structures, designed on REDS base, allow the control of all defects $\equiv 0$, $\equiv 1$, using of only two stimulating-vectors. Diagnosis of singular constant defects $\equiv 0$, $\equiv 1$ of combinational circuits(CC) requires about $2*n$ stimulating vectors, where n represents the number of primary inputs of the circuit. The cost of these facilities is doubling the number of active components on a chip and including of 2 pins in order to guarantee the reconfiguration of the verified structure. In case of a CC generalized model - including of 2 more pins in order to "homogenate" an arbitrary CC with different parities of the convergent signals.

Key words: Design, testability, elementary, reconfigurable, structure

INTRODUCTION

In the last 30-40 years an important attention is being paid to solve the problem of design for testability (DFT)of digital structures and, especially, of CC. The desired properties of a testable circuit were settled: structure with no fan-outs, minimal and complete set of tests, mutual adaptability of the tested circuit and of the testing means, comfort and easiness of testing, "price" of testing improvement comparing to the obtained performance etc.

1. EXPERIMENTAL

The complexity of VLSI circuits has significantly increased the need for design for testability [1] Reddy [2,3] has defined an easily testable network as one having the following properties:

(1) small test set; (2) contains no logical redundancy; (3) structure of the test set is such that it is both easy to generate and integrated the results; (4) faults locatable to the desired degree; (5) test set can be derived without much extra work, either during the design phase or after the network is

defined. This list is qualitative only, but for the purpose of this paper it will serve as a working definition for "easily testable" circuits. Various other properties [3] may also be desirable and can be added to the list: (6) final gate-count should not be excessively high compared with a "normal" implementation; (7) minimum number of additional primary control inputs and observable output used to enhance testability. Trying to be impartial we will make a short review of the actual state of DFT problem solving, evaluation that was made by the world recognized experts.

1.1. Analysis of design for testability concepts for combinational circuits

Developing and organise of testable combined circuits means to increase the number of input and output pins, choose the method of syntheses and a base of logical operations, what is increased the complexity of circuit develop. This is the cost of simplification of testing procedures.

1.1.1. Method Reddy

Theoretical base to choose logical circuits base to realise the function $F(x_1, x_2, \ldots, x_n)$ [3] is it represent in form of decomposition (Read – Muller Expansion Technique) Reed-Muller:

$$F(x_1, x_2, ..., x_n) = C_0 \oplus C_1\tilde{x}_1 \oplus C_2\tilde{x}_2 \oplus ... \oplus C_n\tilde{x}_n \oplus C_{n+1}\tilde{x}_1\tilde{x}_2 \oplus C_{n+2}\tilde{x}_1\tilde{x}_3 \oplus ... \oplus C_{2^n-1}\tilde{x}_1\tilde{x}_2...\tilde{x}_n, \quad (1)$$

where $C_i \in \{0,1\}$, $i = \overline{0,2^n - 1}$-constant; $\tilde{x}_j \in \{0,1\}$, $j = \overline{1,n}$ correspond Boolean variable x_j or $\bar{x}_j$, but not both in same time.

Disadvantaging of this method is growing complexity of realisation circuits and a number of logic levels, which influence technical characteristics [4].

1.1.2. Three-level OR-AND-OR technique

The method is applicable only to positive unate logic functions and produces three level OR-AND-OR implementations in witch every distinguishable fault is locatable. The main trouble at these methods is strict limitation of type realisation function.

1.1.3. Use of additional control logic

Testability of CC depends in direct mode by controllability (C) and observability (O) [2]. These characteristics may be ameliorate by introduce supplementary gates in scope growing number of entrees and out. These technique premise to modify CC and obtain sets that contain only five tests, that allow detection all errors CC [3,5].

1.1.4. Adding test points

Numerous ad hoc designs for testability of VLSI have evolved over the years[1]. Included in these techniques are concepts such as adding test points to increase C and O[4,6]. But the additional pins reduce significantly the utile volume of the chip and, consequently, the technologity of VLSI.

1.1.5. Programmable logic modules

Reconfigurable circuits always have important place in synthesis of easy testable structures. In [6] its describe four logical programmable modules (PLM) types its intended using in synthesis process of digital circuits with increased testability.

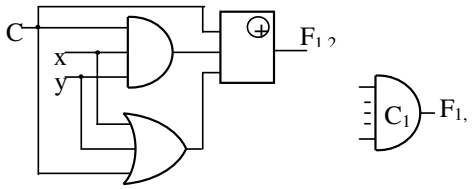
2. RESULTS AND DISCUSSION

2.1. Design for Testability of CC based on elementary reconfigurable digital structures

The utilization of reconfiguration for the purpose of improving the testability of CC was proposed in [7]. One of the ways of Design for Testability of CC is connected with the elaboration of elementary reconfigurable digital structures (ERDS), an elementary circuit for changing parity (ECCP) of binary signal and a generator of successions for determinist signals. In [7] dual ERDS (DERDS) were proposed, in [7] complementary ERDS (CERDS) were proposed, in [7] proposed were the concepts of the organization of extratestable CC. Two logical parts with the same number of inputs are called dual if the signals at their outputs are reciprocally opposite for every combination of input signals. For instance, CERDS of $F_{1,2}$ AND/OR is shown in fig. 1, its functioning being described by Boolean function (b) and table 1.

Table of function CERDS

x	y	C	F_1=x y	F_2=x∨ y	$F_{1,2}$=F1⊕F2 ⊕C
0	0	0	0	0	0
0	1			1	1
1	0			1	1
1	1			1	1
0	0	1	0	1	0
0	1		0		0



$F_{1,2} = Cxy \oplus (C \vee x \vee y) \oplus C$,

a) b)

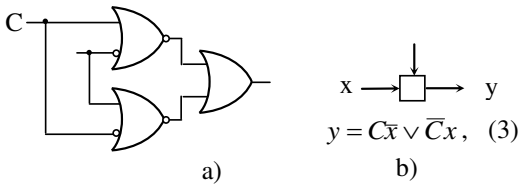
Fig.1. CERDS of $F_{1,2}$ (a) and the symbol of representation (b)

elementary circuit for changing parity (ECCP) [7] and the symbol of its representation are shown in fig. 2. its functioning being described by FB (2) and table 2.

Table 2

Table of function ECCP

C	x	a	b	y
0	0	0	0	Repeat x
0	1	1	0	
1	0	0	1	Inverse x



$y = C\bar{x} \vee \bar{C}x$, (3)

a) b)

Fig.2. ECCP (a) and the symbol of representation (b)

Design for testability will consider in base FB described by expression (4) and contain next steps:

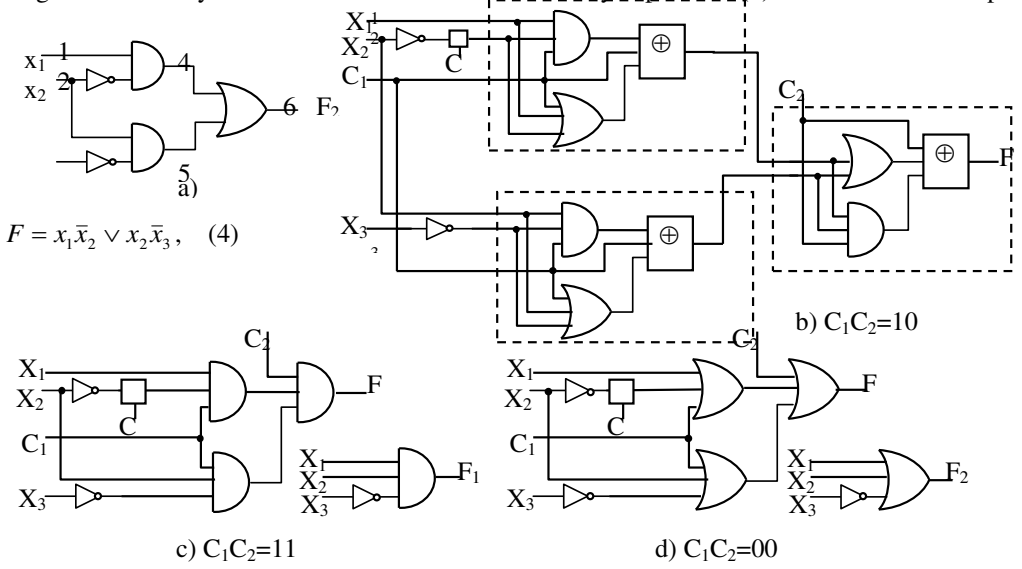


Fig 3. Initial circuit (a), normal function form (b), test regime 1 (c), test regime 2 (d).

1º. Analyzing expression (4) rendering that she contain only gates AND, OR (fig. 3,a)

$$F = x_1\bar{x}_2 \vee x_2\bar{x}_3, \quad (4)$$

2º. Select from multitude CERDS structure $F_{1,2}$=AND/OR, for gates from other logical levels.

3º. Synthesize circuit with CERDS (fig. 3,b).

4º. Analyzing the present counter-claim fan-out with different parity of signals. One these input is input x_2. For assured change input x_2 parity in testable form we place one ECCP after inverter, signal c=0 that don't influence input signal x_2 (in normal ruining process), but c=1 in testable form invert supplementary signal on output, inverter on connection x_2.

5º. In normal mode inputs $C_1C_2 = 10$, that conduced on activate gates 4_1, 5_1 and 6_1.

6º. In testable mode 1 $C_1C_2 = 11$ fig. 3,c, that conduced on reconfigured structures in to maximal degenerate circuit of type AND, equivalent with gate AND with same number of inputs. Verifications all errors ≡0 of inputs gate AND it make with only one test - 111…1, inverting only inputs where stand the inverter.

7º. In testable mode 2 $C_1C_2 = 00$ fig.3,d, that conduced on reconfigured structures in to maximal degenerate circuit of type OR, , equivalent with gate OR with same number of inputs.

Verifications all errors ≡1 of inputs gate OR it make with only one test - 000…0, inverting only inputs where stand the inverter.

3. CONCLUSIONS

1. No matter there is the number of gates inputs and number and type of gates, for presenting fan-outs with diverse gates for CC control, *two* tests are sufficient.
2. No matter there is the number of inputs, type of initial CC gates and number *n* of inputs of arbitrary CC, diagnosis of any constant error requires just *2·n* stimulating vectors.
3. Such concepts for development of Design for Testability are valid also for the arbitrary circuits with reconvergent fun-outs with different parities and initially synthesized in any basis of Boolean operators.

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