THE SYSTEM WITH RECONFIGURABLE ARCHITECTURE FOR SOFTWARE TESTING FOR MCS-51 MICROCONTROLLERS

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ABSTRACT

In this paper the multi-user system design with reconfigurable architecture for testing of MCS-51 software, which excludes listed lacks is considered. This can be achieved because the testing system is developed as WWW of the application. The access to the system is realised by Internet using graphic interfaces for computing structure configuration, editing and analysis of execution result of a programme code.

The system structure is developed as a reconfigurable architecture, which provides switching to input-output ports of an MCS-51 of various external blocks, generation of input signals or ensuring working load for the system. External blocks connection and data transfer direction is realised using architecture configuration program.

Load, compilation and program start of MCS-51 code is realized automatically at data requirement from the Internet user. At occurrence of load or compilation errors of a program code, the message to the user with indication of a place of occurrence of error is generated.

The application provides creation of own and common libraries of a configuration architecture and program codes MCS-51.

The result of execution of a program code MCS-51 is represented to the user as the tables or diagrams in real time. The way of representation of result gets out by the user.

INTRODUCTION

One of the main design stages of control systems on the basis of microcontrollers MCS-51 is software testing in conditions close to real ones. Such conditions can be created only at physical realization of the system and connection of corresponding input and output signals. With the purpose of maintenance of convenience and efficiency the specialized interfaces allowing

interactively to develop and test the software of microcontrollers [1, 2, 3] are developed. Drawback of the given systems is necessity for own interface for each user and functional orientation of the interface to a concrete scope that makes them expensive and inefficient in operation.

In work designing the multi-user system with reconfigurable architecture for testing the software of microcontrollers of family MCS-51 is considered. The system excludes the listed drawbacks and allows the development off new opportunities in the field of interactive programming. The purpose is achieved by developing of the testing system as WWW appendices. Access to system is carried out through Internet technologies with use of graphic interfaces of the user for a computing structure configuration, editing of a program code and analysis of a program code performance result.

BLOCK DIAGRAM FOR MCS-51 SOFTWARE TESTING SYSTEM

Figure 1 shows the block diagram for MCS-51 software testing system, where:

DB – users databases for registration and storage of personal and common libraries of user's program codes;

Web Application – database Web and CGI applications;

MCS-51 – the microcontroller of family MCS-51;

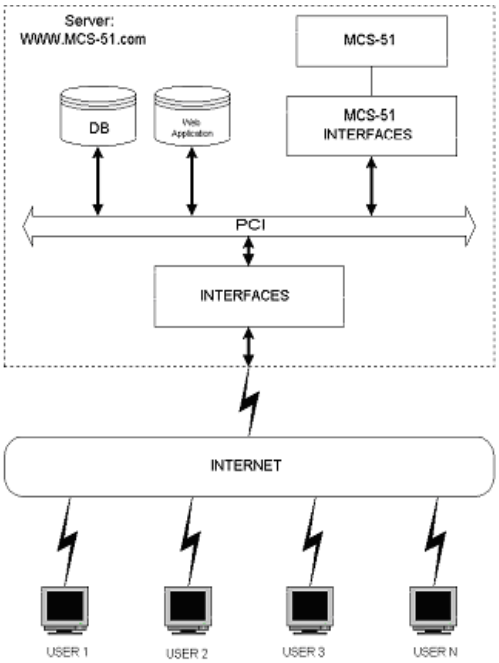

Figure 1. Block diagram for MCS-51 software testing system

MCS-51 Interfaces – the interface of a configuration structure of MCS-51;

PCI – a system bus;

Interfaces – the Internet interface;

Internet – a global network;

User –Internet users.

3. INTERFACE BLOCK IAGRAM

Figure 2 shows the block diagram of the device interface for testing MCS-51 software, where:

PCI – PC bus system;

IPC – bus shapers and tools for adaptation of the interface to system bus PCI;

MCS-51 BUS – an internal bus of the interface with tools for functional blocks addressing;

Rg CONF – configuration registers of computing architecture;

RAM DATA – operative memory of the processed data;

RAM PROG – operative memory of tested program codes;

RAM OUT – operative memory for results storage;

RAM IN – operative memory of data input;

SIS – the block of standard sources of external signals for generation of sequence of codes of standard functions: SIN, COS, TAN, ATAN, etc;

RAM I/O – operative memory of input-output operation through a serial port.;

Rg INT – the interruption requests register;

Rg SYN – the register of synchronization that defines the works frequency for microcontroller MCS-51;

MCS-51 – the MCS-51 family microcontroller;

Port 0 – the standard port of 0 microcontroller, dedicated for performance of operation of data exchange, generation of address and input-output space;

Port 1 – the standard port of 1 microcontroller, dedicated for generation of address space and input-output operation;

Port 2 – the standard port 2 microcontroller, dedicated for performance of input-output operations;

Port 3 – the standard port 3 combined with control signals of the microcontroller dedicated to control and synchronize input-output operations and for data input-output;

Port INT – inputs of signals of external requests of interruption;

Port I/O – signals of data input-output in serial code;

Port SYN – signals of external synchronization of the microcontroller;

CM – computing architecture configuration circuit is dedicated for switching corresponding blocks to ports' inputs of the microcontroller. As switch boards bidirectional multiplexers and demultiplexers are used.

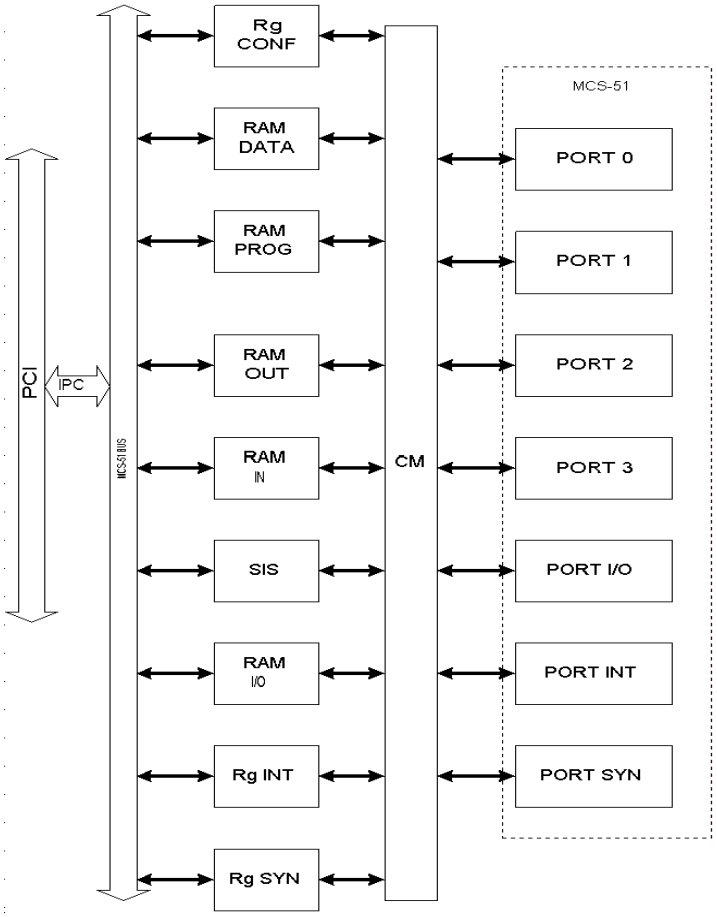

Figure 2. Block diagram of the device interface.

Interface description. Through system bus PCI the processor writes down and reads out the data in / from the interface.

The configuration of the computing system architecture is carried out by record of a configuration code in configuration registers Rg CONF. Thus corresponding external blocks and devices are connected to microcontroller MCS-51 (to input-output ports). The user through the graphic configuration interface defines the structure of the computing system.

In memory RAM DATA the data for processing is written. In memory of program code RAM PROG the program code for testing is written. In memory RAM OUT zeroes are written. In memory RAM IN the data for input ports is written. The block of standard input signals SIS is configured on generation of a corresponding input signal with corresponding parameters. In memory RAM I/O the data for input port in a serial code and zeroes in memory for output port in a serial code is written. In register Rg INT the requests of external interruption is written. In register Rg SYN the code of the frequency generator of the microcontroller synchronization is written.

After computing structure configuration the microcontroller is translated by a signal of synchronization in a mode of performance of a program code. The microcontroller reads out codes of the program, from memory RAM PROG and performs them, addressing to corresponding input-output ports.

After performance of a program code the central processor reads out results from memory RAM DATA, RAM OUT, RAM I/O and transfers them to the user through Internet.

TESTING SYSTEM ALGORITHM

Figure 3 shows the algorithm of program code testing, where:

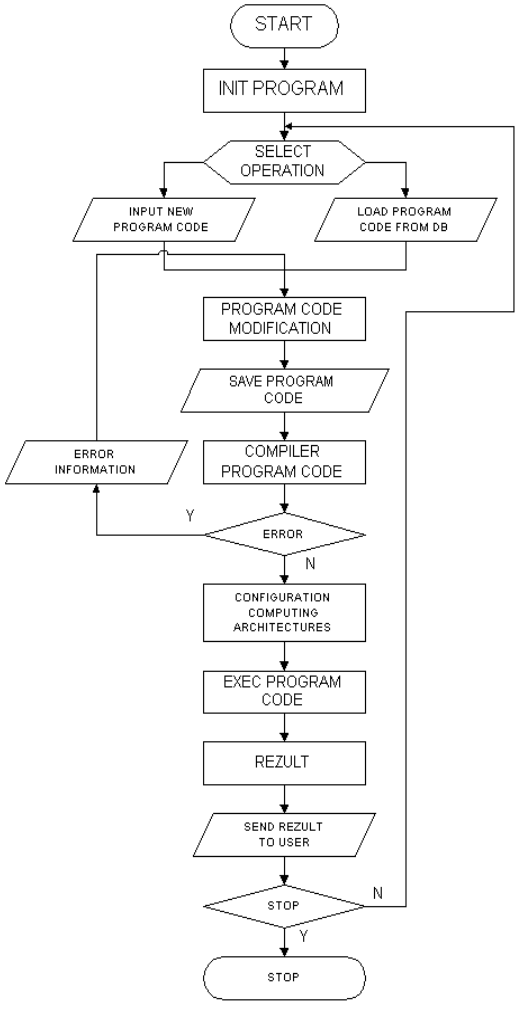

Figure 3. Algorithm of program code testing

START – the beginning of algorithm;

INIT PROGRAM – access program initialization to the resources of program code of MCS-51 testing system;

SELECT OPERATION – a selection of input operation of a new program code or loading of a program code from a database;

INPUT NEW PROGRAM CODE – input of a new program code for testing;

LOAD PROGRAM CODE FROM DB – loading of a program code from a database;

PROGRAM CODE MODIFICATION – input or change of a program code;

SAVE PROGRAM CODE – load of a program code in a database;

COMPILER PROGRAM CODE – compilation of a program code;

ERROR – revealing of mistakes in a program code;

ERROR INFORMATION – the message for the user about mistakes in a program code;

CONFIGURATION COMPUTING ARCHITECTURES – a configuration of

computing architecture for program code testing;

EXEC PROGRAM CODE – performance of a program code of MCS-51microcontroller;

REZULT –the result of performance of a program code in memory;

SEND REZULT TO USER – transfer of a program code performance results to the user;

STOP – check of the end of algorithm;

STOP – the end of algorithm.

In figure 4 the user interface of the microcontroller architecture configuration is presented.

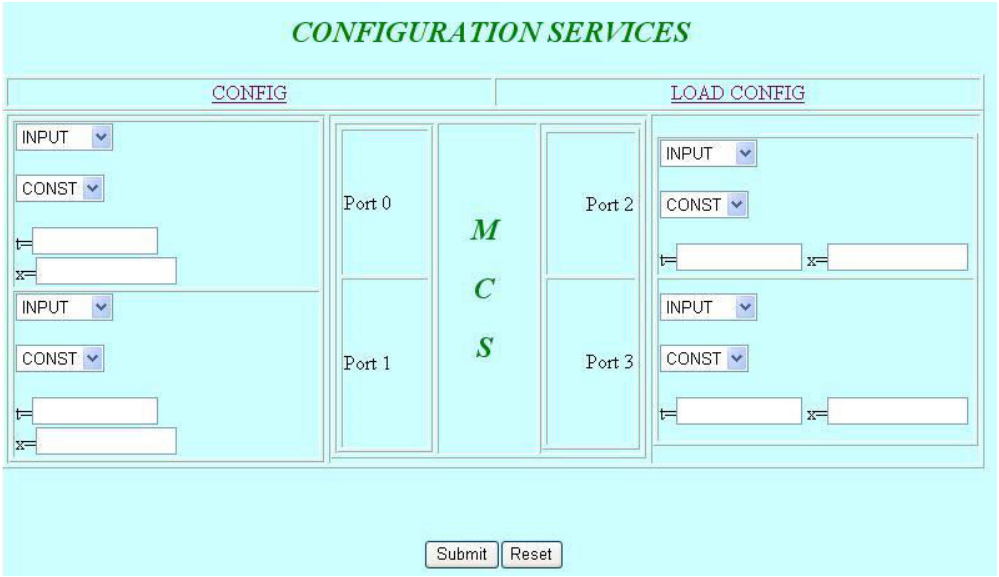

Figure 4. The User Interface of microcontroller architecture configuration

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[3]. http://www.intel.com.