IEEE, SOI-3D-Subthreshold Microelectronics Technology Unified Conference (S3S),
Rohnert Park, CA, USA, 5-8 Oct. 2015

# Monolithic 3D layout using 2D EDA for embedded memory-rich designs

Ionica Pletea, Ze'ev Wurman, Zvi Or-Bach, Victor Sontea

**DOI:** 10.1109/S3S.2015.7333518

## Abstract:

Monolithic 3D integration has generated considerable interest in recent years due it its inherent capability of supporting heterogeneous devices, and its rich vertical connectivity allowing for increased integration while reducing wire-length and power. Few commercial EDA 3D tools are in existence and prior work focused on partitioning logic between two or more logic strata, capitalizing on harnessing existing 2D tools into 3D flows through scripting and other strategies. In this paper we present a methodology intended to exploit the memory-rich nature of modern designs that have large fractions of their area dedicated to multiple memory blocks, and leverages 3D stacking to partition the design into memory-optimized and logic-optimized strata using commercial Synopsys 2D EDA tools.

## References:

**1.** Z. Or-Bach, "The monolithic 3D advantage: Monolithic 3D is far more than just an alternative to 0.7x scaling", *3DIC*, Oct. 2013.
Show Context View Article Full Text: PDF (954KB) Google Scholar

**2.** P. Batude et al., "3D sequential integration opportunities and technology optimization", *IITC/AMC*, May 2014.
Show Context Google Scholar

**3.** M. Ebrahimi et al., "Monolithic 3D Integration Advances and Challenges: From Technology to System Levels", *S3S*, Oct. 2014.
Show Context View Article Full Text: PDF (416KB) Google Scholar

**4.** S. Bobba et al., "CELONCEL: Effective design technique for 3-D monolithic integration targeting high performance integrated circuits", *ASP/DAC*, 2011.
Show Context Google Scholar

**5.** S. Panth, K. Samadi, Y. Du and S. K. Lim, "Design and CAD Methodologies for Low Power Gate-level Monolithic 3D ICs", *ISLPED*, Aug. 2014.
Show Context Access at ACM Google Scholar

**6.** K. Arabi, K. Samadi and Y. Du, "3D VLSI: A Scalable Integration Beyond 2D", *ISPD*, Mar. 2015.
Show Context Access at ACM Google Scholar

**7.** Apr. 2015.
Show Context

**8.** E.J. Marinissen, B. Prince, D. Keitel-Schulz and Y. Zorian, "Challenges in embedded memory design and test", *DATE*, Mar. 2005.
Show Context Google Scholar