HETEROGENOUS INTEGRATIONS ON 3D INTEGRATED CIRCUITS

I.-M. Pletea*, V. Șontea
Technical University of Moldova, D.Ghitu Institute of Electronic Engineering and Nanotechnologies, Chișinău, Republic of Moldova
*E-mail: ipletea@etti.tuiasi.ro

The strongest value of an Integrated Circuit is the integration of many functions in one device. This is and will remain the most important driver of Moore's Law because by integrating functions into one Integrated Circuit we achieve orders of magnitude benefits in power, speed, costs and reliability [1]. 3D Integrated Circuit enables far more than an alternative for increased integration. It provides another dimension of design flexibility [2]. A well-known aspect of this flexibility is the ability to split the design into layers which could be processed and operated independently, and still be tightly interconnected – especially for monolithic 3D [3].

The most important market for semiconductor products is smart mobility. For this market the System on Chip device needs to integrate many functions. In most cases the pure high-performance logic would be about 25% of the die area, 50% would be memories and the rest would be analog functions such as I/O. In 2D they all need to be processed together and bear the same manufacturing costs and limitations. In a monolithic 3D-IC stack using heterogeneous integration each stratum is processed in an optimized flow, allowing for a significant cost reduction and increased functionality [4,5].

The function itself could be constructed better using heterogeneous integration. In many cases only portion of the logic needs to be high performance while other portion could be better and cheaper done using older process node. Other scenarios could include designing different strata with different supply voltages for power savings, different number of metal interconnect layers, or other variations of the semiconductor manufacturing space [6].

3D monolithic device would be a good fit to platform-based designs wherein some part of the device is used by all customers and others are tailored to a specific customer segment. Although there are EDA tools for 3D IC on the market, built on existing 2D tools by adding 3D awareness capabilities, no EDA tools for monolithic 3D exist. There is a need for monolithic 3D EDA Tools with 3D routing, placement, and floor planning tools that work Inter-Layer Vias close to minimum lithography feature size and support both block-level and gate-level partitioning [7].

[1] G.E. Moore. *Solid-State Circuits Society Newsletter* **11** (2006), 33-35
[2] H.B. Muhibul. *SEU Journal of Science and Engineering* **11** (2017), 28-42.
[3] Y. Xie, J. Cong, S. Sapatnekar. Three-Dimensional Integrated Circuit Design. *Springer (*2010)
[4] S. Bobba, A. Chakraborty, O. Thomas, P. Batude, T. Ernst, O. Faynot, G. Micheli. *Asia and South Pacific Design Automation Conference* (2011), 337-343.
[5] C. Chiang, S. Sinha. *Asia and South Pacific Design Automation Conference (*2009), 429-436.
[6] D.H. Kim, S.K. Lim. *Interconnect Technology Conference, IEEE (*2011)
[7] I. Pletea, Z.E. Wurman, Z. Or-Bach. Monolithic 3D layout using 2D EDA for embedded memory-rich designs. *IEEE*. (2015), 1–2.