Two Simple Examples for the Micro-nano Integration of Nanowires as Electronic Device Elements

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***Abstract* – As a part of the conference talk about the mass fabrication and applications of nanostructures, the aim of this paper is to review and compare two approaches for the simple fabrication and integration and of nanostructures into Si-based microchips. The purpose of the integration is the utilization of the different and advanced electronic properties of nanowires. The first method is based on a fracture approach, that integrates nanowires bound to a Si substrate between micro electrodes. These are arrange in a horizontal manner, the second approach allows to integrate free standing nanowires and even 3 dimensional nanowire networks in the chip. As an example for the electronic properties of the nano-micro integrated structures the UV light sensitivity is sown here.**

***Index Terms* – nanowires, nanostructures, Si-based nanochips**

I. INTRODUCTION

One dimensional (1D) metal and semiconductor structures have gained significant research interest due to their different, partially advanced properties originating from effects like a high surface to volume ratio or quantum mechanical influenced properties dominating low dimensional materials, become the important components of micro and nanoelectronic devices [1]. In the past 15 years, significant progress in synthesis and characterization of nanostructures is done, applicability was typically demonstrated by connecting nanowires with techniques like EBL, FIB or direct connections with scanning probe tips revealing suitability of nanostructures in electronic and optoelectronic devices [2].Various methods such as templates [3,4,5], solution growths [6], vapor-liquid-solid (VLS) and its modified versions [7,8,9] as well as several others have been used to synthesize 1D structures. However, easy fabrication routes allowing the integration of nanowires into standard lithography are not yet well established. An optimal integration route should add minimal additional fabrication steps and be compatible with the standard micro processing.

II. NANOWIRE FORMATION AND INTEGRATION APPROACHES

One approach called "fracture approach" is based on a thin film fracture approach [10,11,12], the other one is based on a modified VLS process allowing a bridging of the contacts through interpenetrating junctions [13], will be called here "penetration approach".

In general, the fabrication of the nanowire within the fracture approach microchips contains 5 steps, compare [14] and see figure 1. As first step, Shipley 1813 photoresist is spin coated in a thickness of ~560 nm thickness on silicon substrates of 76 mm-diameter with <100> orientation and a p-doping resulting in a resistivity of 1-10 Ωcm. Please note that the 380 μm thick wafers are top terminated with a 100 nm thick thermally grown insulating SiO2. In a second step, a mould for micro contact lines and the nanowires will be formed. Conventional photolithography is used to microstructure the photoresist. The main step for the nanowire template formation is the exposure of the samples to thermal cycling down to cryogenic temperatures in order to induce the stress in the photoresist thin film resulting in thin film cracks in the photoresist with nanoscopic openings (~100 nm). By using the described pattern with parts of the photoresist that are 200 μm long and 10 μm wide, the fracture pattern forms a highly reproducible well defined 'zig zag' pattern of cracks. The third step contains the deposition of metals or semiconductors by sputter deposition or another a PVD-process in high or ultra high vacuum. This deposition covers the whole wafer surface including the cracks. A deposition of material in the dimensions of about 50-100 nm nominal thickness with an adhesion promoter underneath (thin layer of Ti or Cr) forms nanowires in a reliable manner in the crack. Too high amounts will lead to an overfilling, too small amounts in a dissentious chain of clusters. Please note that the cracks have a relatively high aspect ration of 5-7 which reduces the amount that will be deposited into the crack up to a factor of 10. In contrast, the nominal thickness will be reached in the lithographically formed openings that form the connectors to the nanowires. The fifth final step is the lift off to separate the superfluous metal on top of the photoresist from the microstructured contacts grown in the openings formed by lithography and the nanosized wires formed within the thin film cracks. This photoresist mask lift off was performed by first soaking the sample in acetone for about 1 minute and then keeping it in an ultrasonic bath for roughly 2 seconds. Keeping the sample for long time in an ultrasonic bath may destroy the nanowires.

Vapor-liquid-solid (VLS) or Vapor-Solid (VS) methods are typically utilized to grow free standing nanostructures in a large variety like nano -rods, -wires, -sails, -etc. Usually VLS growth processes can be performed in a horizontal tube furnace equipped with a controlled gas flow control. The needed recipes are the precursor material (typically metalls), catalytic nanoparticles (e.g. gold) and the substrate on which structures will be grown. Experimental variants are

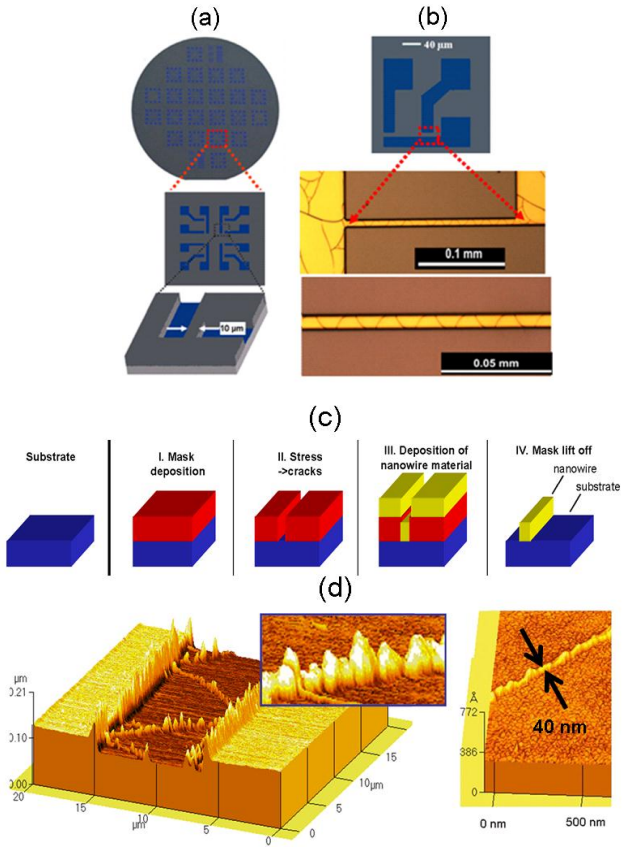

Fig.1. Fracture approach for the fabrication of nanowires with contacts on a Si-chip. a) Photoresist on a Si-wafer is microstructured to form a mold for the later contact lines and a prerequisit for the nanowire formation at the 10 µm wide bridge (magnified). b) The image shows a different view of the bridge used for the nanowire formation. The magnification shows an optical microscopy image of the photoresist in the bridge area after exposing it to thermal cycling that effects the fracture of the thin film. The higer magnification shows the regularity of the crack pattern. c) Schematic overview over the process that is described in the text, resulting in nanowires, represented in d) AFM image of nanowires formed in the 10 µm wide area between the micro contacts. The magnification shows that the wires consist of a chain of clusters.

temperature, gas flow rate and relative source and substrate distances. The growth contains the following 3 steps: (i) During heating in the furnace above the melting temperature of the eutectic, the precursor mixture (ZnO + graphite) transforms into vapor phase and is transported to substrates by carrier gas. (ii) The deposited precursor atoms or molecules form liquid-droplet eutectic alloy with catalytic particles. (iii) Caused by supersaturation, the precursor material is deposited at the interface between the catalyst droplet and its surface. This enables to lift the droplet due to capillary forces and continue to grow nanowires. During cooling the phase separation occurs resulting in formation of 1D rods with catalytic particle on the top [15,16,17]. In typical VLS process, temperature, amount of precursor material, size of catalytic particles and the gas flow rate are the main controlling parameters for growth of 1type of the 1D structure. The nanostructures grow in preferential crystal directions faster than in others, causing the material to shape in a crystalline manner. For the VLS process exists, the here used process doesn't need a catalyst and a tube furnace. A prime example for the nanostructure growth is ZnO. By using the ability of ZnO to interpenetrate during crystal growth, gaps between current lines can be bridged above chips, see Figure 2.

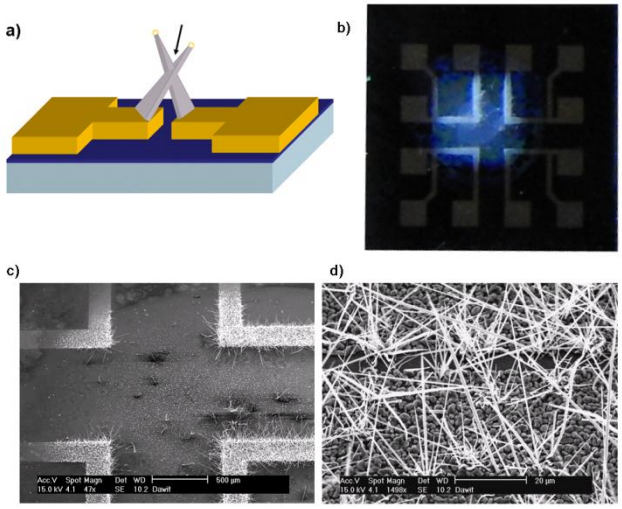

Fig. 2. Growth of three dimensional nanostructures on the current lines of a Si-chip. a) shows the principle, a gap between two current lines can be bridges by growing free standing but interpenetrating nanostructures (arrow point to the interpenetration area). b) Photograph of a 1 cm2 Si chip that is exposed on the area occurring bright with the nanostructure growth conditions. c) This are is shown under the electron microscope where free standing ZnO structures are growing. d) The magnification from c shows the gap between the current lines (darker contrast in the middle) which is bridged by interpenetrating and free standing ZnO structures.

This allows to shape individual nanoscale connectors at specific places on a circuit. A precondition for the integration is the possibility to keep the synthesis temperate on a level that will not destroy already structured electronics. This can be achieved by an active cooling of the silicon substrate or as in our case to lower the process temperature on the chip by shielding all areas where no deposition will take place.

III. EXAMPLES FOR THE ELECTRONIC PROPERTIES:

The above described Nanostructures are already used as gas sensors or field effect transistors, depending on the used metals or semiconductors. It turns out that the nanostructure sensors are advanced in terms of responding pressure and time. A remarkable feature was shown by Penner et al. [18] that is a change in mechanism of a hydrogen sensor. While usually the conductivity decreases with increased hydrogen concentration, the conductivity increases in a Pd-nanowire if they are exposed to hydrogen. This phenomenon could be observed also for gold nanowires integrated by the above described approach [14]. Figure 3 shows the respones of ZnO nanowires formed by the above described methods on chips. In Figure 3a, the fracture approach was utilized and nanowires were formed from sputter deposited ZnO. For comparison, the response shown in 3b originates from free standing interpenetrating ZnO structures. The viewgraph shows a fast response in both cases, however, differences are characteristic for both fabrication procedures. As a general tendency, polycrystalline wires are faster and more sensitive. The grain boundaries between the particles are important sensitive elements that enlarge the effective surface of a nanowire.

IV. CONCLUSION

The two briefly shown examples for micro nano integration demonstrate a feasibility of nanowire based electronics, especially for sensor applications. In the presentation, further examples for the application of nanostructures will be given based on the large scale

synthesis of nanoscale building blocks into macroscopically expanded 3 D networks.

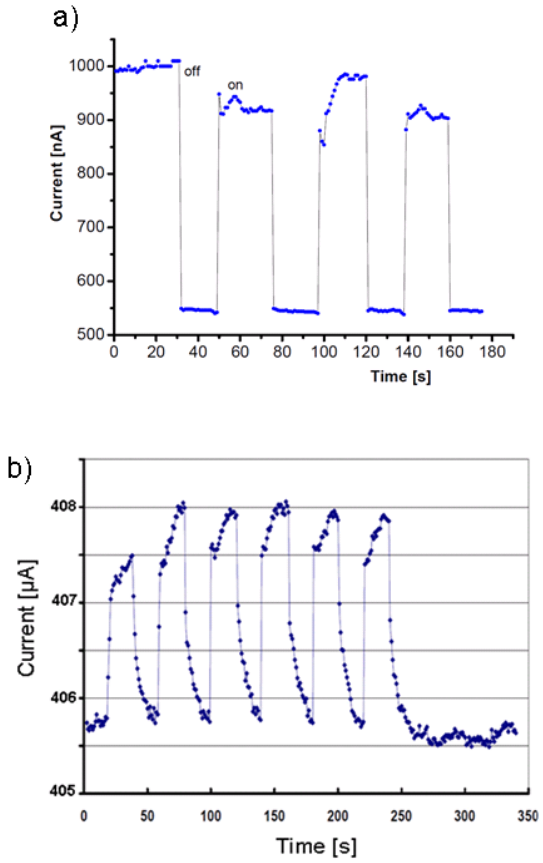

Fig. 3. Response to UV-light of integrated nanowires a) nanowires made by the fracture approach, b) free standing nanostructures formed by interpenetration during growth.

Applications include flexible semiconductors and ceramics as well as applications of superhydrophilicity and superhydrophobicity.

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