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SOME RELIABILITY ASPECTS OF MEMS AND NEMS MANUFACTURING

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Abstract. A full understanding of the physics and statistics of the defect generation is required to investigate the ultimate reliability limitations of manufacturability of MEMS and NEMS. In order that the user can include electronic components in circuits to achieve error-free and reliable functional units, assemblies or devices, must he has understood the mode of operation of these components. Only knowledge of their parameters and special properties allows, according to data sheet specifications and manufacturer's documents the optimal components for a specific application, to select. Both for the analysis of electronic circuits and for circuit dimensioning are knowledge of the structure and function of the used components of semiconductor electronics absolutely necessary.

Keywords: *Failure mode, failure mechanism, failure analysis, wafer-level reliability semiconductor, crystallographic defects.*

Introduction

An failure mode (FMo) is the external symptom of the failed product: for example, a bipolar (Bi) transistor has a short circuit between emitter and collector. Why has this happened? Because a physical process (e.g. a diffusion pipe) led to failure, which is the failure mechanism (FM) in this case. So, the totality of physical and chemical processes leading to failure composes the FM.

In all cases, a failure analysis (FA) must start from an FMo, leading to identification of the FM, because [1]:

• Corrective actions for improving reliability by minimising (or avoiding) this FMo can be elaborated only if the FM is well understood. A reliability growth programme is needed, coupled with management strategy change so that more FMos identified during testing actually receive a corrective action instead of a repair [2].

• FM identification is essential for the reliability of accelerated testing because:

– FMs produced by high-level stress cannot be different to those observed during actual service conditions;

– The obtained degradation laws must be extrapolated beyond the time period of the test and the extrapolation must be made separately for each population affected by an FM.

We must also add that some FMs may induce another FM (e.g. corrosion can lead to sticking/binding). Due to the presence of two FMos, the thermal cycle statistical behaviour is described by a bimodal lognormal failure distribution. There are age-related FMs (such as

hot-carrier or metal migration) that limit the long-term performance of the semiconductors; all these FMos are far worse at geometries below 0.25 μm. A methodology based on an early detection system has to be developed, correlated with a library of the cells available for semiconductor designers to include on their designs, in order to provide a measure of safety and assurance that the deployed systems will maintain robust performance while in service [3].

Obviously, this distinction between FMo and FM also works at system level, where an FMo is the wrong operation of one circuit in the system and an FM (identified by FA at system level) might be a design fault, or the failure of a component of this circuit. If this FA is continued at component level, a new FMo is noticed, which is the former FM at system level. So, to find the root cause of a failure, one must go deeper, to the component level, and not stop at the system level. Consequently, the 'real' FMs are only those found at component level. This can be seen by the fact that FA at component level provides detailed explanations not only about the structural degradation processes of the device, but also about the degradation issues of the materials used to build the device (degradations during device processing or later, during device operation). So not only the component level but also the material level is covered implicitly. *This is the reason why in the following only FMs at components level are detailed*.

FMs can be grouped in various ways, depending on the purpose of the analysis performed. According to where in the component they develop, Hakim proposed the following classification [4]: bulk, interface, oxide, metallisation and packaging. Bulk material and interface properties usually define the intrinsic reliability characteristics, while defects establish the extrinsic reliability characteristics.

FMo and FMs at various process steps

The reliability of a product is built during the manufacturing process. This statement seems obvious today, but not many years ago there was a strong belief that reliability was something that could be 'added' to a final product by a clever combination of tests for reliability selection. In real life, in order to achieve a product with a given reliability level, one has to take reliability issues into account even at the design phase and continue to monitor them during the whole fabrication process, because the FMs are initiated at the process steps. Once the final product has been obtained, the only thing that can be done is to eliminate the weak items from a batch of components by an appropriate reliability selection programme (e.g. burn-in). This will improve the reliability of the whole batch, but not the reliability of each item. The only way to produce a component with a high intrinsic reliability is to avoid the FMs initiated during the manufacturing process.

The manufacturing activity of an electronic component has two main phases: the wafer-level ('front-end') process and the assembly ('back-end') process. The failure risks that may arise at the specific process steps of these two phases are detailed below.

Wafer Level

There are two reasons why wafer is the favourite target for FA: *(i)* many interesting physical and chemical phenomena are involved in component degradation and failure and *(ii)* the wafer is a collection of reliability risks, hence almost any process step may induce a new FM or increase the action of FMs induced by previous steps. This is why a huge quantity of literature has been written on this subject and various techniques for wafer-level FA have been developed. For example, optical microscopy, scanning electron

microscopy (SEM), transmission electron microscopy (TEM), voltage contrast, conductive atomic force microscopy (C-AFM), energy-dispersive X-ray spectroscopy (EDX) and Auger microscopy are all used in sample inspection, where the samples are prepared by parallel lapping, focused ion beam (FIB) cutting, x-sectioning, wet etching or HDP dry etching [5].

Since the 1970s, test structures[1] have been used for process monitoring. First, the process is qualified using traditional lifetime tests. Then wafer-level reliability (WLR) fast tests can be used to provide a so-called statistical signature of the process reliability. If the WLR measurements on product wafers show a similar distribution to those observed on the qualification lots, it can be assumed that the reliability of the devices on the wafer will be statistically similar to that observed during the qualification tests. However, if this is not the case then some other FM is probably present and the only way of ensuring reliability is to re-test the batch, using traditional reliability measurements [6].

The WLR concept was refined in the WLR Workshop, organised annually since 1982 by the Technology Associates. Tools to investigate the reliability risks at the wafer level and to monitor the process factors affecting reliability were created. Two examples (from a multitude) of extended services in the field: *(i)* Coventor launched *Coventor Catalyst*, which is a design for manufacturability (DfM) methodology for developing micro electromechanical systems (MEMS) to ensure optimal manufacturing yield [7]; *(ii)* Dolphin Integration issued a catalogue of test-structure generators, branded RYCS generators, offering a wide range of test-structure kinds [8]. WLR aims to detect potentially unreliable devices and to avoid delivering them to the customer. This requires appropriate measurements done quickly, so that potentially every wafer can be tested, and also that the measurement does not damage the adjacent product devices. Some examples are: hot-carrier measurements, passivation and interconnect dielectrics, gate oxide integrity [9], stress migration, via voiding, current crowding and junction spiking. The four main WLR tests are described in Table 1.

The typical FMs induced by various process steps for the fabrication of an electronic component are presented below. They have been grouped around the four most important subjects from the standpoint of reliability: semiconductor-related FMs, oxide-related FMs, metal-related FMs and FMs related to other wafer-level processes (diffusion, implantation, etc.).

Semiconductor

A semiconductor is a material that has an electrical conductivity between that of a conductor and that of an insulator, which is generally in the range 10^{3}...10^{-8} S/cm. It is an appropriate starting material for modern electronic components.

Today, silicon (Si) is still the most important semiconductor support for electronic components. A huge quantity of scientific work has been reported on this material over the last 40 years. However, other semiconductor materials are being used more and more, such as gallium arsenide (for very high-frequency components) and indium gallium arsenide, gallium phosphide and lead sulfide (for optoelectronic components).

As a starting material in most microchip fabrication, single-crystal Si is processed in wafers, with a diameter that has increased steadily from less than 50 mm in the 1970s to 300 mm today and possibly to 450 mm in the near future. Wafer flatness is an important feature, because it directly impacts device line-width capability, process latitude and yield.

[1] Test structures are chips (or part of chips) specially designed to allow the identification of some FMs and processed in exactly the same conditions as the manufactured product.

The polishing process for Si wafers plays a key role in the fabrication of semiconductors, since a globally planar, mirror-like wafer surface is needed to obtain a good device. The surface roughness of the wafer depends on the surface properties of the carrier head unit, together with other machining conditions such as working speed, type of polishing pad, temperature and down force [10]. Cracks or scratches on the surface of the wafer (usually caused by improper handling) may generate open or short circuits in the electronic components. A careful visual inspection is needed to monitor the surface quality during processing and before sealing. The non-uniformity of the resistivity across the wafer is also a failure risk, because the characteristics of the devices may differ depending on the area of the wafer.

Table 1

Main WLR tests for general applications

Test	Possible FM	Test description
Contact integrity test	Aluminum spiking: silicon dissolution into an overlying Al film, followed by Al penetration at contact windows during contact annealing. The dissolved Si precipitates out during cooling, either as Si islands on oxide strips, or as epitaxial Si at contact windows. May result in a total contact occlusion.	Test structures are stressed at high temperature and contact degradation is evaluated electrically at room temperature and in the dark. Contact spiking can be revealed by a severe increase in leakage current, while contact occlusion will reveal an increase in current resistance.
Hot-carrier injection test	For MOS devices, if large electric fields are applied, carriers can gain sufficient energy (namely hot carriers) to create electron–hole pairs by impact ionisation on the Si atoms. Some of the carriers are injected into the gate oxide and may induce interfacial and/or bulk oxide charges. A degradation of the electrical parameters of the device (mobility, threshold voltage and drain current) occurs.	MOSFET parameters are measured, which are directly related to the capability of the process to generate and trap hot carriers. It is also possible to perform an accelerated stress test under the most severe conditions and to compare the result with the characterisation work performed during qualification.
Metal-integrity test	Electromigration (EM) in thin-film interconnection lines: the electron/ion flux induced in metal tracks by high-current densities. The degradation of the conductor is due to the agglomeration of vacancies, which can result in a void through the metal track or in the local accumulation of metal atoms, which can cause a short circuit between adjacent conductor layers.	Wafer-level test SWEAT (standard wafer-level EM accelerated test), based on the acceleration of EM in the metal line by means of a high current density: the metal line is subjected to a constant current stress defined by a chosen acceleration factor and by the maximum temperature that the metal line can reach without activating other diffusion mechanisms.

Continuation Table 1

Oxide integrity test	Oxide dielectric breakdown occurs when sufficient charge is injected into the oxide by forcing a current through the dielectric or by applying a high electrical field. The damage produces structural changes (traps or interface states), which lead to a low-resistance path through the oxide layer and result in a permanent leakage of the dielectric.	For gate-oxide applications, constant voltage stress (CVS) or linear voltage ramp stress (LRVS) are used. For tunnel-oxide applications, current stresses are used, such as constant current stress (CCS) or exponential ramped current stress (ERCS).

The most important characteristic of any semiconductor, as a starting material for a future electronic component, is the number of **crystallographic defects**, which interrupt the regular pattern of atomic arrangement. Basically, the existence of defects in semiconductors is detrimental to the future devices; there are, however, some beneficial effects of electrically active defects, which may be introduced deliberately with the aim of improving the characteristics of the semiconductor. This is called 'defect engineering'. One example is the intentional introduction of oxygen to reduce the radiation-induced formation of electrically active defects [11], which improves the radiation tolerance of the device. Carbon has an adverse effect, as modelled and discussed in [12].

In Table 2 the possible FMs induced by crystallographic defects are shown. The solution for avoiding some of these FMs is to have a rigorous input control of the semiconductor wafers, by using the detection methods indicated in the table. However, to be noted that some of the mentioned defects are induced in the semiconductor structure by various processing phase (oxidation, implantation, diffusion, etc.).

Passivation

Among the solutions for passivation, oxidation is the earliest one, being today the basic steps in the fabrication of any active electronic component, both for bipolar and unipolar (MOS) technology. Because silicon is still the best choice among semiconductors for electron technology, silicon dioxide (SiO_2), with a relative dielectric constant, k = 3.9, is the material of choice for inter-layer-dielectric (ILD) applications. Consequently, many of the silicon-based technologies that have evolved are based on the deposition, patterning and removal of SiO_2 during processing. This material has remarkable properties for device fabrication including exceptional thermal properties, excellent electrical properties and enviable mechanical properties. In almost every important field (thermal stability, breakdown voltage, leakage current, mechanical properties, etc), except for dielectric may be expected to be inferior to SiO_2.

The properties of any low-k materials (with k lower than SiO_2 one) may be expected to be inferior to low-k materials (with k lower than SiO_2 mechanical properties, etc), except for dielectric constant, the properties of any low-k materials crosstalk between conductor lines and signal delays in the back-end-of-the-line (BEOL) interconnect wiring. Two important low-k candidates for replacing SiO_2 are organic polymers and silicates [17].

However, it seems the semiconductor manufacturers have chosen inorganic-like materials, with which they were more comfortable through their experiences with oxide insulators. Consequently, Si-Me containing organosilicate materials (k = 2.7…3.0) have been

developed and are now manufactured for the current 90 nm technology [18]. To be noted that the methyl groups (necessary to provide low dielectric constant properties and hydrophobicity) reduces the density, modulus, hardness and fracture energy [19].

Among the possible failure risks at passivation, one may note the formation of cracks or pinholes (which may lead to electrical breakdown and short circuit) and the non-uniformity of film thickness (leading to the lowering of breakdown voltage and the increasing of leakage current). Also, the crystallographic defects represent significant failure risks. The two most significant defects induced into silicon wafers during oxidation are dislocations and stacking faults [16].

There is a large variety of FMs that could be induced by oxidation. Three typical ones are gathered in Table 3 and will be detailed in the following. Basically, hot carrier injection is one of the causes of interface state generation, but we treated this FM as a different one, because it is one of the most important FM in today MOS devices.

Interface state generation

The imperfections in the oxide (e.g. mobile ions Na^+ and/or K^+, fixed oxide charge or oxide traps), which are the result of poor fabrication processes, may represent a significant danger for the oxide as efficient dielectric, because they could initiated interface states. The induced charge at the interface oxide-silicon and in oxide may alter the flatband voltage. There are at least four distinct types of charges in the oxide-silicon system: *(i)* Fixed interface charge, *(ii)* Oxide trapped charge, *(iii)* Interface trapped charge, *(iv)* Mobile charge resulting from alkali-metal ions, particularly sodium.

But the interface states at the silicon/oxide interface could be generated even by the necessary electrical stress tests. There is still slight stress in the film, and dangling silicon bonds are usually passivated by hydrogen atoms, and are not electrically active. The density of unpassivated silicon dangling bonds is negligibly low, below 10^{10} cm^{-2}.

However, under electrical stress, the weak Si-H bonds may break and interface states are created. Negative bias temperature (NBT) stress is another important cause of interface states generation. The transistor degradation under this mode is called negative bias temperature instability (NBTI), and occurs even when the circuit is in quiescent, if the *p*MOSFET happens to have its gate tied to high voltage. This is one of the most serious reliability concerns of all [20].

Table 2

FMs induced by crystallographic defects

Class of defect	Defect types	Detection methods	Effect (possible FM)
Point defects	*Vacancies* - sites that are usually occupied by an atom but that are unoccupied. If a neighboring atom moves to occupy the vacant site, the vacancy moves in the opposite direction. *Interstitials* - atoms which occupy a site in the crystal	Photoluminescence [13], Optical microscopy [14], Preferential chemical etching and x-ray topography [15]	The presence of point defects is important in the kinetics of diffusion and oxidation. The rate at which diffusion of do-pants occurs is dependent on the concentration of

Continuation Table 2

	structure at which there is usually not an atom. *Frenkel defect* - a nearby pair of a vacancy and an interstitial. This is caused when an ion moves into an interstitial site and creates a vacancy. *Clusters (Swirls)* - formed between different kinds of point defects (e.g., if a vacancy encounters an impurity, the two may bind together if the impurity is too large for the lattice). *Extrinsic point defects* - more critical than intrinsic point defects, point defects involve foreign atoms, which usually come from dopants, oxygen, carbon, and metals.		vacancies. This is also true for oxidation of silicon.
Line defects	*Dislocations* - linear defects around which some of the atoms of the crystal lattice are misaligned: *(i)* Edge dislocations - caused by the termination of a plane of atoms in the middle of a crystal; *(ii)* Screw dislocation - more difficult to visualise, but basically comprises a structure in which a helical path is traced around the linear defect (dislocation line) by the atomic planes of atoms in the crystal lattice. *Dislocation loops* - if the dislocation consists of an extra plane of atoms (or a missing plane of atoms) lying entirely within the crystal. The dislocation line of a dislocation loop forms a closed curve that is usually circular in shape, since this shape results in the lowest dislocation energy.	Transmission electron microscopy (TEM), Field ion microscopy (FIM), Atome probe techniques, Deep level transient spectroscopy (DLTS)	Major role in the fatigue crack initiation phase. Also, they may serve as sinks for metallic impurities as well as disrupt diffusion profiles (this ability may have a beneficial role in the removal of impurities from the wafer (gettering).

Continuation Table 2

Area defects	Grain boundaries – regions where the crystallographic direction of the lattice abruptly changes. This usually occurs when two crystals begin growing separately and then meet. Twins - Electrically quiescent defects that do not introduce large stresses, and, consequently, do not accumulate impurities [16]. Stacking faults - typical defects induced by process phases (e.g. oxidation). The kinetics of growth is related to the local concentration of point defects. These defects are sinks for impurities [16].	High resolution x-ray diffraction, Nomarski microscopy, atomic force microscopy (AFM), Transmission electron microscopy (TEM), Scanning electron microscopy (SEM), high resolution electron microscopy (HREM), Raman and photoluminescence spectroscopy	Most common in EFG Si ribbons, used for manufacturing solar cells. General effects: *(i)* reduce the short circuit current density as a result of a reduction in the minority carrier lifetime; *(ii)* reduce the voltage and the fill factor as a result of the introduction of a high density of space charge recombination centres [16]. Oxidation-induced stacking faults (OSF) may increase the reverse current in *pn* junctions, degrade the breakdown voltage and reduce the gain of biploar devices.
Bulk (volume defects)	Voids - small regions where there are no atoms, and can be thought of as clusters of vacancies. Precipitates – if impurities cluster together to form small regions of a different phase.	Idem	Idem

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Table 3

Main characteristics of oxide-related failure mechanisms

Failure mechanism (FM)	Short description	Possible failure mode (Mo)
Interface state generation	Charges induced at Si-SiO_2 interface and in the oxide may modify the flat-band voltage of MOS devices and increase the leakage in reversely biased bipolar junctions.	In MOS devices, a drift of the threshold voltage occurs due to the modifications of the flat-band voltage. In bipolar devices, the reverse current increases and becomes instable.
Hot carrier effects	High-energy electrons and holes are injected into the gate oxide, near the drain, as a localized oxide-charge trapping and interface trap generation. Hot carrier related degradation can occur in deep submicron devices at drain voltage as low as 1.8 V.	Significant reduction in drain voltage and transconductance, shifts in threshold voltage and decrease in drain current capability.
Dielectric breakdown	Dielectric breakdown is the destruction of a dielectric layer, usually as a result of excessive potential difference or voltage across it, when the electric field strength surpasses the dielectric strength of an insulator. Two phenomena could be involved: *(i)* Breakdown of gate oxide and *(ii)* Time dependent dielectric breakdown (TDDB).	Conductive or short circuit paths through the dielectric or leakage at the point of breakdown.

Interface state generation

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temperature instability (NBTI), and occurs even when the circuit is in quiescent, if the *p*MOSFET happens to have its gate tied to high voltage. This is one of the most serious reliability concerns of all [20].

Hot-carrier effects

The term 'hot-carrier injection' (HCI) describes the phenomena by which the carriers (electrons or holes) under intense electric fields gain sufficient kinetic energy to overcome a potential barrier and to be injected into the gate oxide. The kinetic energy of microscopic particles is directly related to the temperature of the matter they constitute: the higher is the temperature, the higher is the (average) kinetic energy of the particles; hence the word 'hot'.

Studying the degradation and failure phenomena by HCI

HCI occurs as carriers move along the channel of a MOSFET and experience impact ionization[2] near the drain end of the device. The damage can occur at the interface, within the oxide and/or within the sidewall space. Interface-state generation[2] and charge trapping induced by this mechanism result in transistor parameter degradation, typically as switching frequency degradation or breakdown [21]. A high gate voltage can also pull hot carriers into the gate oxide and trap them there before they even reach the drain region. Trapped carriers or charges in the gate oxide can shift the threshold voltage and transconductance of the device. The excess electron-hole pairs created by impact ionization can also increase substrate current, which in gross cases can upset the balance of carrier flow and facilitate latch-up.

There are four known mechanisms for HCI, which describe the conditions for carriers to enter the gate oxide [22]:

• Substrate hot electrons (SHE) - electrons are thermally generated in the substrate and drifted by an electric field towards the interface. The substrate current produced by impact ionization can induce bipolar latch-up in CMOS structures and the hot carriers injected in gate oxide form interface states and trapped oxide charge. In time, this charge causes instabilities and parameter drift. These serious reliability problems are increasing with the decreasing of the device geometries. A correction method is to limit the source–drain voltage to values below the threshold for the generation of hot carriers.

• Channel hot electrons (CHE) - the carriers are traversing the channel, and undergoing a low number of lattice collisions under the influence of the strong lateral electric field;

• Drain avalanche hot carriers (DAHC) - carriers are created in avalanche plasma and undergoing, due to the strong lateral electric field, a high number of impact ionizations; this is the most physically destructive HCI mechanism [23];

• Source side hot electrons (SSHE) - this mechanism gives rise to larger shift of the threshold voltage and larger drift of the saturated drain current [24].

HCI produces non-catastrophic failures, which develop gradually over time and change the performances of the device. The effects of HCI are more prominent in *n*MOS devices compared to the *p*MOS devices, because it requires 3.3 eV for electrons to overcome

[2] Impact ionization occurs when a high voltage is applied across the source and the drain of a MOS device and the channel carriers are accelerated into the drain's depletion region, causing them to collide with lattice atoms that result in electron-hole (e-h) pairs. The displaced e-h pairs are gaining enough energy to propel some of them towards the gate oxide of the device and trap them there.

the surface energy barrier at the $Si–SiO_2$ interface and get injected into the oxide, compared to 4.6 eV for holes. In MOSFET with *p* channel, the degradation is caused by hot carriers injected into the drain side of the gate oxide and the type of trapped hot carrier depends on the bias conditions. Obviously, in MOSFET with *n* channel the degradation is caused by hot holes [20]. HCI occurs in logic circuits in general and not just in RAM cells. When MOS transistors are employed in digital logic, the logic steady states are regions of low stress because there is either a high field near the drain but the gate is low and the channel is off, or the electric field near the drain is low, in both cases leading to no generation of hot carriers. Hot carriers are generated almost exclusively during switching transitions. The effects of the hot-carrier stressing can be determined by measuring a variety of device parameters, including assorted currents, voltages, and capacitances for the device.

Degradation of device characteristics due to hot carriers occurs also in bipolar transistors. This is a well-known phenomenon in which h_{FE} degradation occurs when a reverse bias is applied across the emitter and base [26 - 29]. With the advanced shallow junction devices of recent years, there is a tendency towards increased reverse leakage current between the emitter and base, causing device characteristic degradation to readily occur as a result of the hot carrier effect. A significant increase in minimum noise figure NF_{min} and noise resistance R_n after hot carrier stress (which cannot be explained alone by the change of the carrier density in the inversion layer) was observed [25]. It was demonstrated that the presence of interface states at source side shows much greater impact on the degradation of NF_{min} and R_n. This provides strong experimental evidence that the local noise at source side plays a more important role in determining the channel noise.

Conclusion

When systems are properly designed, components can often be produced to demonstrate near-zero failure rates over their lifetime. The study of degradation and malfunction phenomena is necessary for each case. For systems, assembly and system failures must be examined.

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