Electrical behavior of the CdTe heterojunction cells fabricated on polyimide substrates

Tamara Potlog, Nicolaie Spalatu
Physics Department, Moldova State University, 60, A. Mateevici str., Chisinau, MD 2009
tpotlog@usm.md

Abstract
Hot-wall technique has been used for preparation of CdTe heterojunction cells on the polyimide substrates covered with ITO layer. Carrier transport mechanisms of the heterojunction cells are briefly discussed. It has been established that tuneling recombination current flows through states near or at the interface with a thermal activation energy 0,34 eV; 0,33 eV; 0, 34 eV; for applied bias voltages 0,1V; 0,2 V and 0,3 V; respectively. The reverse current is limited by the carrier generation process.

I. INTRODUCTION

A_2B_6 thin films semiconductors and CdTe in particular, seam to be useful as optoelectronic devices working in the visible wavelength [1-3] and (3-5 mm) IR regions [4]. However, little interest is being shown towards thin films II- VI semiconductors. This is presumably due to the fact that the physics of these materials is not yet completely understood. However, the realization of electronic devices using CdTe requires film deposition on conductive substrates which are polycrystalline semiconductors. The study of the obtained heterojunctions can be useful in obtaining insight junction properties in order to improve heterojunction devices. CdTe films grown on CdS substrates have great interest because of their applicability in solar cells [5-8]. In the present work, ITO/CdS/CdTe heterojunction was fabricated by hot wall technique (HWT) on polyimide substrates. The dependence of the current- voltage (*I-U*) characteristics in dependence of the temperature in both forward and reverse bias was studied in an attempt to obtain information on the transport mechanisms of the devices. In addition, capacitance-voltage (*C-U*) measurements were applied for characterization of these heterojunction cells.

II. EXPERIMENTAL

2.1. ITO/CdS/CdTe heterojunction cells technology

An flexible ITO/CdS/CdTe heterojunction cell has been developed utilizing ITO/polyimide substrate which has an high optical transparency (~85 %) as well as thermal endurance up to 420°C. Both CdS and CdTe thin films were deposited by hot wall technique. The source temperature was T_{ev}=630°C and of the substrate was varied from 100°C to 320°C. The optimum substrate temperature was established for both layers as 310°C±5°C.

The thickness for CdS was about 0, 12 μm and for CdTe layers was approximately ~ 2, 5 μm. After deposition of CdS and CdTe a $CdCl_2$:H_2O annealing at 405°C±5°C for the recrystallization and junction activation was applied. Then the structures were etched in $K_2Cr_2O_7$:H_2SO_4:H_2O. Ni deposited by thermal evaporation was used as an ohmic contact.

2.2. Current-voltage characteristics

The achievement of high efficiency solar cells requires the understanding of the junction transport and loss mechanisms. In order to obtain information on the transport current mechanisms of the ITO/CdS/CdTe devices were measured current-voltage characteristics in the dark in the interval of the temperatures (303-393) K. In heterojunctions, it is well-known that, if the current transport is dominated by a thermal process, the current-voltage relationship takes the form

$$I = I_{OR} \exp\left(\frac{eU}{nkT}\right), \qquad (1)$$

while if tunneling dominates, the I-V relationship has the form

$$I = I_{OT} \exp(AU), \qquad (2)$$

Fig. 1 illustrates the I-U temperature characteristics of ITO/CdS/CdTe heterojunction cell. With the increasing of the measurement temperature as well as forward and reverse current increases. We assume that the curves measured till 363 K temperatures have a behavior as in the case of to systems formed from two junctions switched in series opposite to each other. For the curves measured higher than 363 K at applied biases $U < U_D$ the current is an exponential function of the voltage. When U becomes greater than the diffusion potential (U_D) for the curves measured for temperatures higher than 363 K the I-V characteristics can be approximated by a linear dependence:

$$I = \frac{U - U_D}{R} \qquad (3),$$

where U_D is the diffusion potential equal to the cut-off voltage (U_C) and R is the series resistance of the cell. The rectifying ratio at 1 V for all the investigated devices is varied from 30 to 50. The cut-off voltage is modified with temperature according to the relation

$$U_C(T) = U_C(o) - \alpha T \qquad (4),$$

where $U_C(0)$ - the cut-off voltage at T=0 K, α – is the cut-off voltage temperature coefficient equal to (2, 4) x 10^{-3} V·K^{-1}. This signifies the decrease in the band gap energy of the device due to thermal energy provided by the increase in temperature. and the movement of the level Fermi at the midle of the band gap of the *p* and *n* regions. It can also be seen from Fig. 2 that with the increasing of the measurement temperature the diffusion

potential is decreased. In order to appreciate transport mechanism of the device the logarithm of forward current versus voltage at different temperatures were plotted. Fig 3 shows these dependencies which exhibit two linear regions. The saturation current density I_o is obtained by extrapoliting $ln\ I_f$ versus U curves to zero and the values of n and A are calculated from the slopes. To establish the nature of our I-U characteristics, we have tabulated I_o, n and A for these curves in table 1.

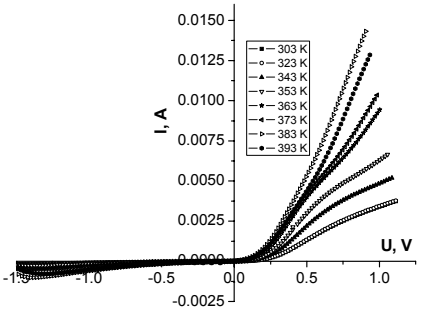

Fig.1. I-U characteristics of ITO/CdS/CdTe heterojunction at different temperatures in both forward and reverse.

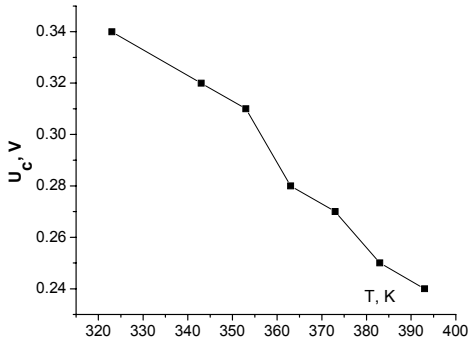

Fig.2 . Dependence $U_C=f(T)$ for ITO/CdS/CdTe heteroiunction cell

Table 1: Electrical parameters of the ITO/CdS/CdTe heterojunction cell

T, K	*α*	*n*	*A*
303	39,03	1,89	8,33
323	41,50	2,07	8,34
343	50,72	1,59	8,36
353	47,98	1,67	8,13
363	39,82	1,62	7,35
373	34,97	1,61	7,20
383	31,06	1,67	6,96
393	29,43	1,61	6,94

In case of our structures const. A changed relatively slowly as a function of temperature as shown in the table 1. Figure 4 illustrates the forward $ln\ I_o(T)$ at various bias voltages. As one can see there exists a temperature low-bias voltage current governed by the relation (2), where $ln\ I_o$ varies approximately as the temperature T. These results can be qualitatively explained as a tunneling-dominated current due to carriers from the valence band of the p-type material or the conduction band of the n-CdS tunneling into interface states where they recombine.

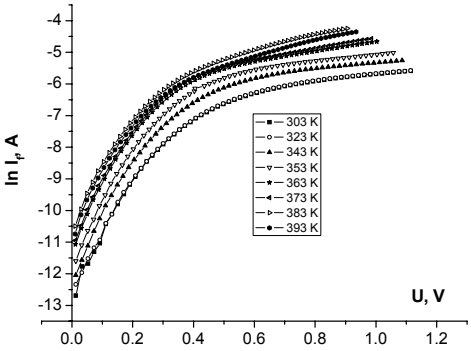

Fig.3. Semilogarithmic plot of forward bias of I-U curves for ITO/CdS/CdTe heterojunction cell at different temperatures.

At bias voltages $0,25\ U<U<U_D$ for $T>363$ K are ploted dependence of $ln\ I_{oR}$ as a function of $1/T$ at various bias voltages.The ideality factor n varies from 1,6 at 393 K to 1,9 at 303 K. The I_0 is found to vary according to the relation

$$I_0 \sim exp\ (-\Delta E_{af}/kT) \qquad (5),$$

where the ΔE_{af} is the activation energy of the charge carriers in the forward bias. This region corresponds to a recombination-limited current. The activation energies obtained at various bias voltages shown in Fig.5 constitute 0,34 eV; 0,33 eV; 0, 34 eV; for applied bias voltages 0,1V; 0,2 V and 0,3 V; respectively.

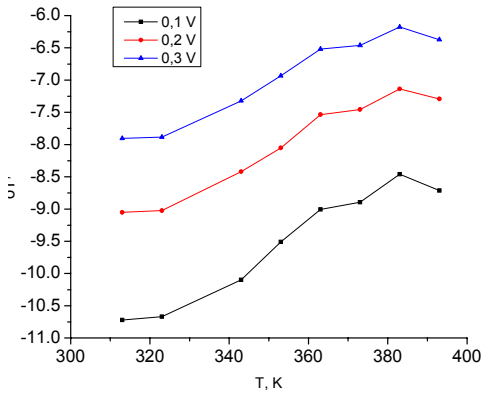

Fig. 4. Temperature dependence of the tunneling saturated current intensity I_{oT} of the ITO/CdS/CdTe heterojunction cell at various bias voltages.

We have used a model devised by Donnelly and Milnes [9] which combines tunneling to interfaces states and recombination at these states to fit experimental results. We attribute the activation energy to thermal activation of holes below the hole quasi-Fermi level in CdTe to an energy at which two conditions are simultaneously satisfied; (1) the barrier is thin enough for appreciable tunneling to occur and (2) the concentration of inteface states and their effective recombination cross sections are high enough for appreciable recombination to occur.

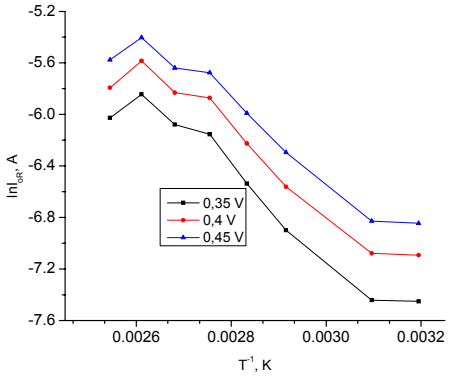

Fig. 5. Temperature dependence of the recombination saturated current intensity I_{OR} of the ITO/CdS/CdTe heterojunction cell at various bias voltages.

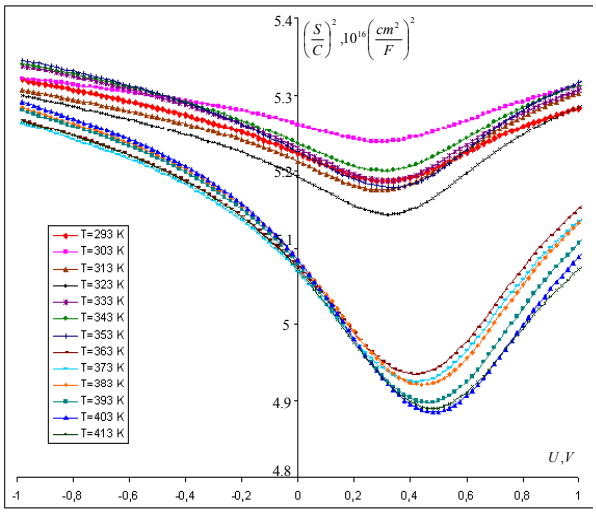

Fig. 6. Plot of $(S/C)^2 = f(U)$ for ITO/CdS/CdTe heteroiunction cell in both forward and reverse bias.

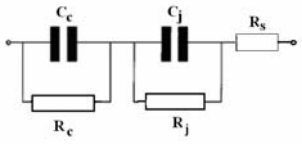

Fig 7. The equivalent circuit for the model of the ITO/CdS/CdTe heterojunction cell.

Assuming that the current is described by an interface recombination limited mechanism, we can write,

$$J_R = q\bar{S}_i N_b \exp(-\frac{q\Delta E_0}{kT}) \exp(\frac{qU}{nkT}) = J_{R0} \exp(-\frac{q\Delta E(U)}{kT}) \quad (6),$$

where S_i is the interface recombination velocity, N_b – is the doping in the base, and ΔE_0 is the thermal activation energy for this process. If equation (6) is valid, the slopes of $ln\ I_R$ versus 1/T curves will be bias dependent and ΔE_0 will be related to the observed slopes $\Delta E(U) = \Delta E_0 - (U/A)$. The values of $\Delta E(U)$ and ΔE_0 for these devices are in good agreement for the temperature regions in which this interpretation of the $ln\ I_f$ versus U characteristic appears to be valid. On the other hand, the dependence of the reverse current intensity on 1/T leads to the value of the activation energy 0,59 eV at 0,2 V, which is different from the obtained value of ΔE_{af} for the forward bias. This indicates that the reverse current should be limited by the carrier generation process.

2.3. Capacitance-voltage characteristics

In order to discuss the transport mechanism, it is important to measure the ionized impurity concentration of the carriers; by means of capacitance-voltage measurements. Fig.6 shows the C^{-2}-U characteristics of ITO/CdS/CdTe heterojunction cell. The capacitance was measured using a small a.c. voltage of 1 MHz. As a rule, interface states result in formation of double regions and in accordance with the Anderson model heterostructure can be represented as two Schottky diodes switched towards each other [10]. Equivalent electric circuit of the heterojunction is shown in Fig. 7. The five components in this circuit are voltage- and frequency-dependent and capacitance can be rather complicated function of bias voltage and frequency. An analysis of this circuit for zero series resistance is given in [11]. Because of R_s toghether with differential resistance of each diodes governs the distribution of applied voltage it can influence both current-voltage and capacitance-voltage characteristics. This seems to be the reason why the dependence of the capacitance on the bias voltage is rather weak in the heterostructures investigated, Fig.6. One can estimate high-frequency capacitance from the formula [11]

$$C = \frac{C_{CdS} C_{CdTe}}{C_{CdS} + C_{CdTe}}, \quad (7)$$

where C_{CdTe} and C_{CdS} are the capacitances of appropiate diodes. It is clear that $C_{CdTe} >> C_{CdS}$ and $C \cong C_{CdTe}$. At zero bias C_{CdTe} can be calculated from the relation

$$C_{CdTe} = \left[\frac{q\varepsilon_o \varepsilon n}{2U_D}\right]^{\frac{1}{2}} \cdot S \quad (8)$$

It was established that the impurity concentration is of (8-9) 10^{13} cm^{-3}. Another explanation of the data analyzed above consists in existence of intermediate layer at the interface due to interdiffision of tellurium and sulfur atoms. One can suppose that interdiffusion results in formation of CdSTe solid solution. Obviously, its energy gap should be higher as well as value of $\frac{\partial E_g}{\partial T}$ should be lower than in the CdTe. The obtained data supports this supposition. So to clarify experimental results additional investigations are needed.

III. CONCLUSION

It has been demonstrated that CdS/CdTe heterostructures can be grown by hot-wall tehnique on polyimide substrate covered with ITO layer. The investigations of the dark current-voltage and capacitance-voltage characteristics lead to the conclusion that the characteristics exhibit a recombination dominated tunneling current.

IV. REFERENCES

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