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Fault Models for Phase Change Memory

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***Abstract*—Phase Change Memory (PCM) is the newest type of non-volatile memory that shall replace the currently wide spread flash memory. Recent research activities performed on PCM reliability and operation have identified special failure modes that are particular to this type of memory. In this paper, these failures are identified and their behavior is analyzed in order to develop appropriate fault models that describe their behavior using traditional memory fault notation. In addition, an efficient test algorithm, called March-PCM, is proposed to test all modeled faults.**

Index Terms— Algorithm, fault models, March test, Phase Change Memory.

I. INTRODUCTION

Different memory technologies have different features that are normally emphasized in a particular technology such as Static Random Access Memory (SRAM), for example, is used when high performance is needed. On the other hand, due to their cost-effectiveness, DRAMs are used when high capacity is favored over performance. When non-volatility is required, flash memory is considered the best available choice when compared to other types of nonvolatile memories in terms of cost and performance [1]. In recent years, the interest in Chalcogenide based PCM has increased significantly. This can be seen over the past five years by the exponentially increasing number of patents for this technology. PCM is believed to be the memory that will replace all other types of memories used nowadays due to its many desirable characteristics [1-3]. These features include high performance comparable to SRAMs, small size analogous to DRAMs, and non-volatility but without the limited endurance as the case in flash.

PCM is a novel non-volatile semiconductor memory concept that utilizes phase transitions in a thin-film chalcogenide material, such as $Ge_2Sb_2Te_5$ (GST), to store data information [2,4,6]. Chalcogenide material can exist in two stable states with either high or low resistance value. High resistance state is known as amorphous phase (or RESET state) whereas low resistance state (or SET) is known as the crystalline phase. The resistance of the amorphous state is approximately two orders of magnitude larger than that of the polycrystalline state [3,4]. The transition from one state to the other can be accomplished by heating the chalcogenide material.

Many researchers have been performing technology characterization studies on PCMs to assess their performance [8-10]. Reliability studies have shown that PCMs exhibit failure modes that are particular to this type of memory [10-11], however, limited number of studies targeted the development of fault models for these failures [12].

Manufacturing test is an important part of any digital system production cycle and in order to develop efficient tests for PCM, analysis of the different failure modes must be performed and appropriate fault models must be developed. The objective of this paper is to discuss some of the issues associated with phase change memory test. The first goal for this paper is to discuss PCM cell structure and their principle of operation. The second goal is to describe the various failure modes known for PCMs and develop appropriate fault models to model them. The development of a test algorithm for PCM using the proposed fault models constitutes our third goal.

This paper is organized as follows. Section II overviews PCM cell structure and its theory of operation. Different failure modes and the proposed fault models are discussed in section III. A Test algorithm for PCM faults and its detection capabilities as compared to previously developed algorithms are described in section IV. Section V concludes the paper and highlights future work.

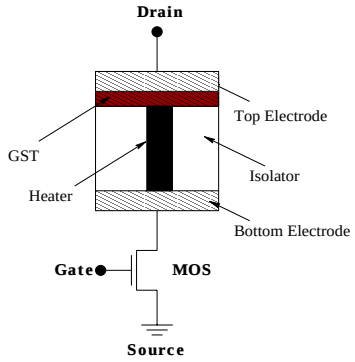

Figure 1: Cross Section of PCM Cell

II. PHASE-CHANGE-MEMORY

The PCM cell consists of a chalcogenide layer (i.e. GST), a heater, and a select transistor. Figure 1 shows a typical cross section of a PCM cell based on a design that utilizes MOSFET as a select transistor [1,3,6,8,10]. Phase of the GST material can be changed from crystalline to amorphous

(or vice versa) through current or plasma heating. Plasma heating is the method used in optical memories such as CD-R and DVDs whereas current heating is utilized in PCMs. The crystalline state is used to identify a cell with a logic value "1", whereas an amorphous state represents a logic "0".

The amorphous phase is accomplished by heating the material above melting temperature (T_m) then cooling it rapidly below glass transition temperature (T_g). Heating the material between T_m and T_g causes nucleation and crystal growth to occur over a period of several nano seconds which results in the crystallization of the GST material. Typical melting temperature of commonly used chalcogenide glasses is about 600 C^o whereas glass transition temperature occurs at about 300 C^o [3]. The programming time for amorphous phase is done in about 10ns while crystallization of the GST requires approximately 50ns. Figure 2 shows the I-V characteristic of the GST material along with typical read voltages and programming currents of typical PCM cell. The GST material in poly-crystalline state behaves as a quasi-linear resistor, while it behaves as voltage snapback at a voltage V_T in the amorphous state. Programming or writing the memory cell is accomplished by applying a voltage above V_T whereas reading requires a value lower than V_T [6,10]. The material of the cell switches to low resistance value without any phase transformation at voltage above V_T. When the applied voltage is reduced below the holding voltage (V_H), amorphous or crystalline resistance value is restored. Therefore, to ensure correct sensing of the store information in the cell, read voltage is normally below V_H.

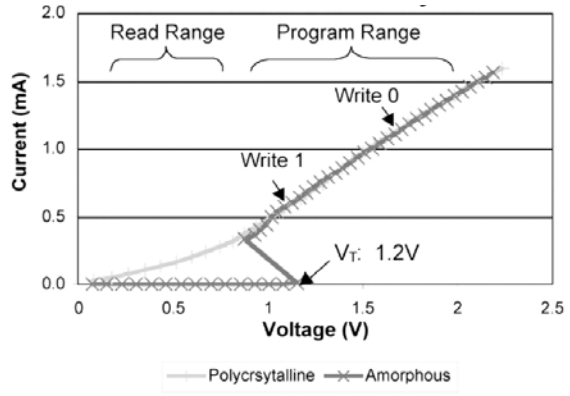

Figure 2: IV Characteristics of PCM Cell [10]

Figure 4 shows the connectivity of a typical PCM memory cell array. The PCM cell can be modeled as a MOSFET with a variable resistance connected to its drain terminal. The drain of the cell is connected to the bitline (BL), gate terminal is connected to the wordline (WL), and source terminal is connected to ground. In such memory array, the reset/set operation (writing logic "0"/"1") is accomplished by applying appropriate high voltage (value depends on the value to be written) on the BL and turning on the pass transistor by applying appropriate gate. Current following through the cell will either, melt the GST material, hence writing value "0", or it will heat it between T_m and T_g thus resulting in writing logic "1". As for the unaddressed cell during programming, their BL and WL are grounded.

During read operation, appropriate voltage is applied to the addressed cell BL and the pass transistor is turned ON. The low voltage on the BL is required to provide the necessary read current and avoid the un-intentional modification of the stored data in the addressed cell. The stored data is sensed by measuring the amount of current passing through the cell's BL. For example, to read a cell, the BL is biased with read voltage (i.e. 0.4V) and the addressed cell is selected by applying a voltage, above the pass transistor threshold voltage, on the cell's WL. A cell in the amorphous phase will be highly resistive hence, no current (or extremely small current) will pass through the cell and majority of the current will flow in the BL. The amount of current that flows in the BL is sensed by a sense-amplifier and is compared with a reference current. When the magnitude of the current flowing in the sense amplifier is greater than that of the reference cell, the cell identified to have a logic "0" value. However, in the case where the GST material is in crystalline state, considerable current will flow through the memory element, hence minimizing the amount of current flowing through the BL. The sense amplifier will sense a current with a magnitude that is less than the reference cell, hence concluding the content of the cell to be logic "1".

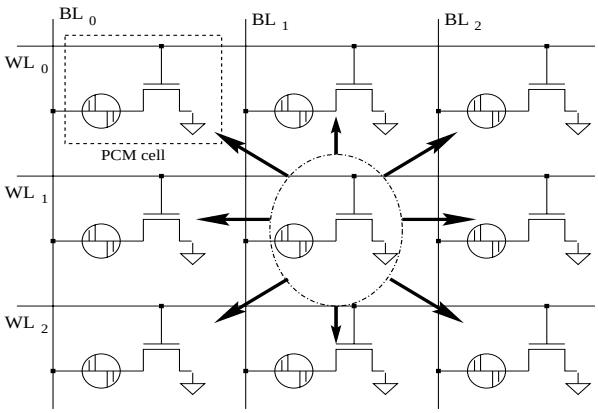

Figure 3: PCM Memory Array

III. PCM FAULTS AND DISTURBS

During initial design phase of a new product, the technology undergoes a tremendous amount of characterization testing to evaluate design alternative, process quality, as well as performance characteristics. However, due to the manufacturing environment, spot defects as well as other anomalies would result in defective parts. In this section, possible PCM memory failures will be briefly discussed and appropriate fault models that can be used to describe the faulty behaviors of these failures.

A. PCM Disturb Faults

In non-volatile memories, writing data to memory cells requires either elevated voltages as the case in flash memory, or elevated currents, hence temperature, as the case in PCM [13]. High voltage/current results in behaviors known as disturbs. Disturbs are simply defined as the unintentional change in the content of an un-addressed cell while operating on another. It is also possible to observe disturbance on addressed cells as the case in read disturb faults[8,10,12]. Manufactures normally spend considerable time to optimize the design of the memory cell and array organization to reduce these unwanted effects.

PCM operations are based on the generation of heat to store information in memory cells. Therefore, the design and implementation such memory must guarantee proper isolation of individual cells. Furthermore, current/voltage rating during the various operating modes must be within design limits to guarantee proper operation and data retention characteristics. If any of these requirements is violated, disturbs or data retention failures might occur.

The first type of disturbs, which is considered as one of the most pronounce failure mode, is called proximity disturb (PD) and is also known as program disturb [12,14]. This failure can be explained as the unintentional loss of stored information when a cell in its immediate proximity (first neighbors, as shown in Figure 4) is being programmed to a RESET state (logic 0). This failure mode is caused by thermal cross-talk generated while programming. For example, if a cell is undergoing a RESET program operation (writing "0"), the GST material is heated to its melting temperature to program appropriate information into the addressed cell. On other hand, the generated heat could be dissipated to neighboring cells, due to defects or improper isolation, which could lead to the loss of stored data (due to GST crystallization) in the neighboring cell. In [14], authors have shown during RESET program operation, first neighbors experience elevated temperatures hence increasing the probability of proximity disturb. In was shown in [14] that the temperature in the disturbed cell is a function of the technology node, cell structure, and isolation method used. Therefore, it is important to test for this type of faults to guarantee the compliance of the implemented design with all aspects of the design specifications. This type of disturb can be modeled as an idempotent coupling fault of type $<xw0;0/1_m/->$. The fault type is given using traditional coupling fault notation $<S_a;S_v/F/R>$, describing a fault involving two memory cells, an aggressor cell (a) and a victim cell (v) [15]. In this notation, $S_a \in \{w0,w1,r0,r1\}$, is the operation sequence of the aggressor (selected cell), S_v operation sequence/initial state of the victim (affected cell), $F \in \{0,1\}$ is the state of the faulty cell, and $R \in \{0,1,-\}$ the output of the read operation. The value "-" in field R is used when the operation performed is a write operation. Note that in the PD fault primitive, the subscript "m" represents the fact the cell's resistance is not a typical one, it is rather less resistive, thus referred to as marginally RESET. The subscript signifies special detection requirements such as margin read operation [13]. The characteristics of margin read operation will be discussed in section IV. Such failure can be avoided by properly controlling heat generation and confinement within the active GST material of the core cell by various isolation methods and cell heater design [14].

The second type of disturb failures is known as Read Recovery Disturb (RRD) [11]. This type of failure occurs when reading a cell immediately after it has been programmed to high resistance state (RESET). The read operation returns a value "1" whereas the true value of the cell is actually logic "0". This failure occurs due to the fact that the newly programmed cell is in non-equilibrium state and additional time is required for free carriers to recombine/diffuse to restore equilibrium after removing programming voltages. In [11], the authors had shown that the drift dynamics of the resistance can be explained by time evolution of resistance as:

$$R(t) = Rd(t) \,||\, R(0)\, e^{(t/\tau)} \quad (1)$$

where Rd(t) is the drift component of the resistance, R(0) is the resistance at time zero in the recovery transient, and τ is the effective recombination time for access carriers. It has also been shown that in addition to resistance recovery, there is also threshold dynamics (V_T) that occur [11]. These findings necessitate proper design read operation voltages and timing. Since this behavior is an intrinsic to all PCM cells, this failure mode is not a memory cell array fault, rather it is considered as a read circuitry fault. However, the behavior can be modeled as a memory cell array fault as it is normally done for peripheral circuitry faults [15]. This failure can be modeled as a class of Incorrect Read Fault (IRF) of type $<1w0R0/0/1_m>$. Unlike the previous fault which requires two cells (aggressor and victim), this fault is a single cell fault (same cell is an aggressor and a victim).

Another type of disturb that occurs under low current condition is read disturb (RD) [7]. This disturb behavior is similar to read disturb faults that occurs in Flash memory which is limited to cells high V*T* state (in PCM it is the amorphous state). During read operation, the amount of current flowing through the cell is in the order of 1μA. When defects are present, the amount of current flowing in the cell is increased leading to increase in the amount of heat generated in the GST material. If the amount of current flowing in the GST layer results in localized heating, some parts of the GST material will switch from amorphous to crystalline state [8], thus destroying the stored information in the cell. This fault can be modeled as a fault of type $<0r0/1_m/0>$. Read disturb fault of this category can is also known as Deceptive Read Disturb Fault (DRDF) [15]. It is assumed in this fault model that the read operation is short enough to read the cell in the correct logic state before switching occurs. Note that the fault primitive again uses subscript "m" to signifies marginal RESET resistance. The reason for marginal resistance value is that the localized

heating crystallizes only a small portion of the programmable GST layer. Thus, the total resistance of the cell is the parallel combination of the amorphous and crystalline GST material resistance which is less than that of a typical amorphous phase. Due to the decreased resistance, this fault type also requires special read operation similar to that used for RRD fault.

Another read disturb phenomenon is observed in PCM which is NOT observed in flash memory is called "false write" (FWR). In such disturb, the read operation changes the addressed cell from a SET to RESET state. This fault can be view as the complement of the RD fault described above. In [10], it was shown that this failure occurred due to the false activation of write current circuitry during read operation. Therefore, this kind of failure is categorized as a peripheral type of failure but can be mapped into a memory cell array fault as it was the case for RRD fault. Thus, this fault can be modeled as deceptive read disturb fault (DRDF) of type <1r1/0/1>. Again, the assumption here is that the read operation is short enough for the sense amplifier to recognize the switching, thus the cell's original value is read.

B. Other PCM Specific Faults

In the previous section, we discussed faults that unintentionally alter the content of a certain cell (whether addressed or non addressed) which are normally referred to as disturb faults. In this section, we discuss more general failure modes that can occur in PCMs. Unlike the previous kind of failures, this kind of failures normally result in permanent faulty behavior. In the former type of faults, the correct behavior of the cell is restored data is re-written into the cell (i.e. PD fault) or sufficient time is allowed before reading (i.e. RRD fault). However, the faults discussed in this section normally result into a faulty behavior that cannot be corrected by any means. The first type of failures in this class can be attributed to the overheating of the GST material during programming (due to high current magnitude). When the generated heat is extremely high during programming, the chalcogenide material might intermix with the adjacent material of the core cell thus destroying its physical characteristics [8]. In such circumstances, the cell will continuously exhibit low resistance value that can no longer be altered. This failure mode is known as Stuck Set (SS) due to the fact that the faulty cell will permanently have a stuck-at value. However, since this type of failure will not occur unless the cell is programmed to the RESET state at least once, thus this failure mode is modeled as a transition fault of type <↓/1>.

Another failure mode in this category is called Incomplete Program Fault (IPF). This fault occurs when the cell is undergoing a RESET operation and it final resistive state is less than that of a typical cell [16]. In severe cases, the cell exhibit a resistance value close to that of a cell in the SET state. Even if resistance value is few K-ohms from SET value, such cells pose a reliability concern and might result in in-field failures. The cause of this behavior is attributed to the presence of contaminants and other impurities in the active region of the GST material. These impurities results in parallel conductive paths with low resistive characteristics hence reducing the overall resistance of the cell. Another cause for this behavior can be attributed to variation in the crystallization rate of the GST material which is normally circumvented by fast quench time [17]. This failure mode can be modeled as a $<\forall /1_m>$ fault which requires a margin read operation to be detected as a stuck-at fault.

The final failure mode of PCM cells addressed in this discussion is called "Stuck Reset" (SR). Even though this failure more has only been observed during cycling, hence not a manufacturing related defect, we are including it here for the sake of completeness. Such failure mode occurs after extensive cycling, where the GST material of the PCM cell might become separated from its top electrode leading to an open circuit at the contact region [1]. Since such failure occurs only if the cell is programmed to RESET state at least once, then it can be modeled as a transition fault of type <↑/0 >.

Table II summarizes the names as well as the fault models associated with various failure modes of PCM memories. In the next section, we proposed a test algorithms that detects the various PCM faults.

Table I: Specific PCM Fault Primitives

FAILURE	CAUSE	FAULT MODEL
PD	Thermal Coupling	$< xw0; 0/1_m/- >$
RRD	Read Access Timing	$< 1w0r0/0/1_m >$
RD	Localized heating	$< 0r0/1_m/0 >$
FWR	Read/Write Circuitry	$< 1r1/0/1 >$
SS	Over heating	<↓/1>
SR	Over heating	<↑/0>
IPF	Contaminants	$< \forall/1_m >$

IV. EXCITATION CONDITIONS AND TEST ALGORITHM

In the previous section, different fault models for each failure mode particular to PCM were discussed. Even though the excitation conditions for each fault can be deduced from it fault primitive, we explicitly state them along with the detection conditions of each fault and is given in Table III. The table specifies the type of fault, victim cell initial state, excitation operation, and detection condition. Note that in the last column, detection conditions are represented as three possible cases. The first case labeled as "Rx" means that fault detection requires performing a read operation expecting value "x". Moreover, when symbol "Rx_m" is used, it signifies that the fault can only be detected by a margin "x" read operation. The used of rounded brackets, i.e. "(margin)", signifies a conditional need for a read operation to detect the fault. In such case, a

read operation is not required if margin read operation is used in fault excitation part. Otherwise, an addition read operation (margin read) is needed.

Table II: Excitation and Detection Conditions

FAULT	STATE	EXCITATION	DETECTION
PD	0	$W0_{neighbor}$	$R0_m$
RRD	1	W0,R0	($R0_m$)
RD	0	R0	$R0_m$
FWR	1	R1	R1
SR	0	↑	R1
SS	1	↓	R0
IPF	X	W0	$R0_m$

A. Excitation and Detection Conditions

Starting with PD fault, this fault involves two cells, an aggressor cell and a victim cell. The victim cell must be initially in the RESET state (logic 0). In order to excite this fault, a neighboring cell must be programmed to RESET state (labeled as $W0_{neighbor}$ in the table). The final state of the victim cell is changed from RESET to SET and thus detected by a R0 operation. On the other hand, fault RRD is excited by writing 0 followed immediately by reading the same cell expecting a 0. The R0 operation in the excitation sequence is used to detect the fault, hence, no additional read operations are required for fault detection. As for RD and FWR faults, both of these faults are excited by a read operation. The difference between these two faults is the initial state of the faulty cell and the fact that the RD fault requires a margin read operation to detect this type of fault. Margin read operation used different reference current value than that used during normal read operation. Only one margin read operation is needed to detect special requirement PCM faults. This margin read is called RESET margin read (i.e. $R0_m$). The difference between the normal read and the margin read is the reference current used to identify the stored information in a cell. Since the faulty cell's resistance value is marginally different that a typical cell, the reference current should be designed in such a way that it distinguishes between faulty and fault-free cell. For example, a typical RESET cell will conduct a current less than 1μA during a read operation whereas a cell that is SET conducts a current in the range 50-100μA. Thus, a typical read reference current is chosen to be around 20μA. Therefore, for a marginally RESET cell, margin read reference current (I^{RST}_m) can be chosen to be approximately 5μA. Using margin read operation, cells that conduct current in excess of 5μA will be considered as SET whereas those that conduct less current are considered as RESET. The characteristics of the margin read reference current with respect to the normal level is graphically depicted in Figure 4.

As for SR fault, it can be excited by writing 1 to the cell and is detected by read 1 operation, whereas SS fault is excited by writing 0 and is detected by read 0 operation. Similarly, IPF is excited by write 0 operation and detected by margin read 0 operation ($R0_m$).

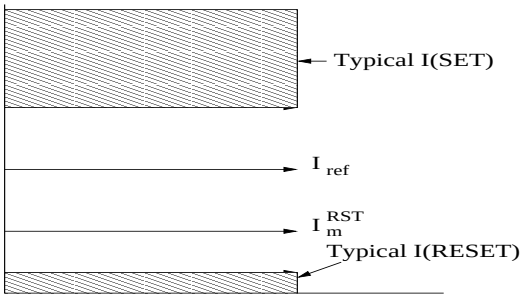

Figure 4: Margin Read Reference Currents

B. Test Algorithm

After considering the various conditions for fault excitation and detection, we developed a March algorithm that can detect PCM specific faults in addition to other common faults such as stuck-at (i.e. SA0 and SA1) , address decoding (AF), and Transition faults (TF). Algorithm March-PCM is given below:

March-PCM= {M0:⇳(W0); M1:⇧ ($R0_m$;W1); M2:⇩ (R1); M3 :⇩(R1;W0;$R0_m$); M4 :⇩ ($R0_m$)}

The algorithm is given using conventional notation of a March test. A March test consists of a sequence of march elements where each march element by itself consists of a sequence of operations that are all applied to a given memory cell before proceeding to the next one. The way to proceed to the next cell is determined by either increasing (⇧) or decreasing (⇩) address order. An increasing address sequence starts with address 0 and ends with address *N-1* for a memory containing *N* addressable cells (bits, bytes, or words), whereas a decreasing address sequence starts from *N-1* and terminates at 0. If the addressing sequence can be arbitrary, the symbol '⇳' is used. Operations on memory cells are 'w0' (write value '0'), 'w1', 'r1' (read the cell expecting '1'), and 'r0'. The complete March test is delimited by curly brackets '{…}', while a march element is delimited by regular brackets '(...)'. Different march elements within a test are separated by semicolons, whereas different operations within a single element are separated by commas [15]. For example, a march element such as ⇧(r0,w1,r1) performs a read '0' followed by write '1' followed by a read '1' operations. If we assume that the cell that underwent the pervious operation was *i*, then the next cell to be addressed will be the cell *i+1* since the address sequence is designated with '⇧'symbol.

In order to ease the understanding of the workings of the algorithm, we have labeled each march element with a label, i.e. Mx, where x ∈{1,2,...etc}. For example, M1 in algorithm March-PCM refers to march element ⇩(W0;R0). Moreover, March-PCM algorithm utilizes margin read operations such as "$R0_m$" which signifies that the read

operation uses $I^{RST}{}_m$ (described in previous section) as a reference current value. The following is a proof how algorithm march-PCM detects the various PCM faults described in Table II.

All PD faults except the fault in the last cell (n-1) are excited by W0 of M0 and are detected by $R0_m$ in M1. Fault in cell (n-1) is excited and detected by W0 in M3 and $R0_m$ in M4, respectively. As for RRD faults, they are excited by element $W0R0_m$ of M3 and are detected by $R0_m$ of the same march element. For RD faults, $R0_m$ in M3 excites these faults, and $R0_m$ in M4 detects them. March elements R1 in M2 and R1 in M3 excites and detects FWR faults, respectively. Moreover, IPF faults are excited by W0 in M3 and detected by $R0_m$ in M4. M3 operations W0 and R0 excites and detects SS faults, respectively. As for SR faults, they are excited by W1 of M1 and detected by R1 of M2.

In addition to PCM specific faults mentioned above, March-PCM algorithm can detect other common faults such as Stuck-at (SAF), address decoding (AF), and transition faults (TF). The complexity of March-PCM is 11N where N stands for the number of cells in the memory array. It is clear that proposed algorithm is an efficient algorithm that is capable of detecting all PCM faults.

V. CONCLUSION

In this paper, we have discussed failure modes that are specific to Phase Change Memories or PCMs. We describe the origin of the faulty behaviors and developed appropriate faults models for each behavior. The developed faults models were used to develop a March algorithm (called March-PCM) that is capable of detecting all these faults in an efficient manner. Future work associated with this topic includes the development of electrical model for defective cells as well as the validation of faulty cell behavior by means of electrical simulation.

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