System of Error-Correcting Decoding Based on FPGA

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***Abstract* — This paper presents implementation of error-correcting decoding system, that would allow to increase noise immunity of video data transmission from satellite SATUM to the Earth. Implementation of the system based on FPGA is proposed, which, along with the choice of decoding methods, allows to minimize hardware and time resources, providing a sufficient correcting ability.**

***Key word* — Error-correcting decoding, Reed-Solomon, Wyner-Ash, concatinatated coding, correcting ability.**

I. Introduction

An important objective within the project of Moldavian student's satellite SATUM is elaboration of a system of reception and transmission of video data to Earth. Transmission of video data from a satellite is characterized by the necessity of processing large amounts of data at a high speed. At the same time, the data received from the satellite by the ground station will be distorted as a result of interference in the communication channel, changes during the transmission of channel characteristics, decrease of the signal amplitude etc.

To ensure data transmission with minimal losses it is necessary to provide an acceptable level of error probability. In most cases, an improvement of characteristics of the communication channel are not sufficient. In addition, possibilities of increasing noise immunity by increasing transmission power and spectral width in standard digital data transmission systems are significantly limited. In this case, it is necessary to apply the methods of error detection and correction based on the introduction of informational redundancy in the transmitted message – error-correcting encoding, that allows to detect and correct errors of various kinds [1].

The most complicated is the task of decoding large volumes of received video data in real time mode, which sets significant restrictions (hardware and temporal) on the processing devices and the methods used. This paper presents one of the possible solutions that consists in implementation of error-correcting decoding of data received from the satellite on the bases of FPGA (Field Programmable Gate Array) microchips. The combination of two types of codes (block codes and convolutional codes) allows to provide the necessary correcting ability, while the choice of methods and the use of FPGA chips reduces the decoding time while minimizing the resources used [2].

II. Error Correcting Coding

Error correcting codes can be divided into two major groups – block codes and convolutional codes.

Block codes are codes, in which an information stream is divided into segments and each segment is converted into a block – a sequence of information and control symbols. In these codes formation of control symbols and error detection and correction are performed within each block separately [3].

Convolutional codes form a sequence of symbols that is not divided into separate codewords. Formation of control symbols is performed by the recurrent rules.

Block codes are characterized by their ability to correct burst errors, while convolutional codes efficiently correct single errors. Since in satellite transmission channel may occur distortion of various types (both burst and single), the advantages of various types of codes can be combined by applying the so-called concatenated coding. In this case, information is encoded by one type of code and then the other.

The most commonly used methods of block coding is a Reed-Solomon codes and Hamming codes. Implementation of encoders for these methods are similar. For our purposes Reed-Solomon code was chosen due to the fact, that its correcting ability is higher than that of Hamming code, which makes up for more complex implementation of Reed-Solomon decoder.

The most commonly used method of convolutional coding is Viterbi code, but at the same correcting ability hardware complexity of Viterbi decoder is dozens of times higher than of Wyner-Ash code, which was chosen for elaborated device.

III. Implementation Of Reed-Solomon Decoder

A. Reed-Solomon codes

Reed-Solomon are non-binary cyclic block codes that are able to correct burst errors. They are constructed in polynomial field i.e. extended Galois fields. The encoding process is based on calculation of the remainder of the division of the input data by a generating polynomial.

The codeword can be obtained from the formula: in

$$c(x)=a(x)\,x^{r} + \mathrm{Re}\,st[a(x)/g(x)] \quad (1)$$

where *c(x)* – encoded message;
a(x) – input information;
g(x) – selected generating polynomial;
r – degree of the polynomial g(x).

The most commonly used Reed-Solomon code is RS (20, 16) with 8-bit symbols. Each code word contains 20 bytes, of which 16 are information bytes and 4 – control symbols. In this case, the decoder can correct any of 2 code symbols (bytes) in case if no more than 2 symbols are damaged.

B. Reed-Solomon Decoding

The decoder consists of error syndrome calculation unit (is composed of a Reed-Solomon encoder), error polynomial calculation unit, unit of error location determination, error values calculation module and a module data restoration. Reed-Solomon decoder can be represented as the following block Scheme (Fig. 1).

In figure 1 R(x) – received codeword, Si – syndromes, L(x) – error localization polynomial, Xi - error positions, Yi – error values, c(x) – restored codeword, v - the number of errors.

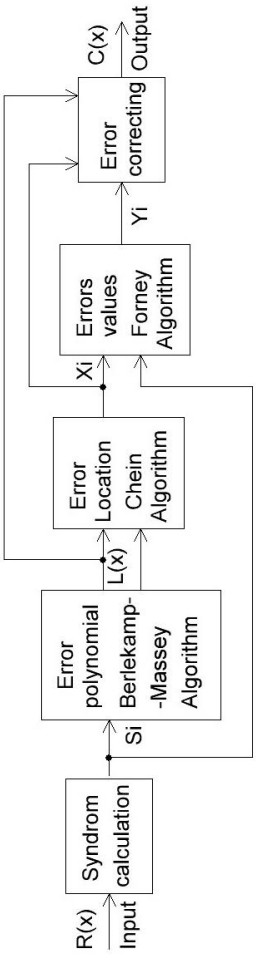
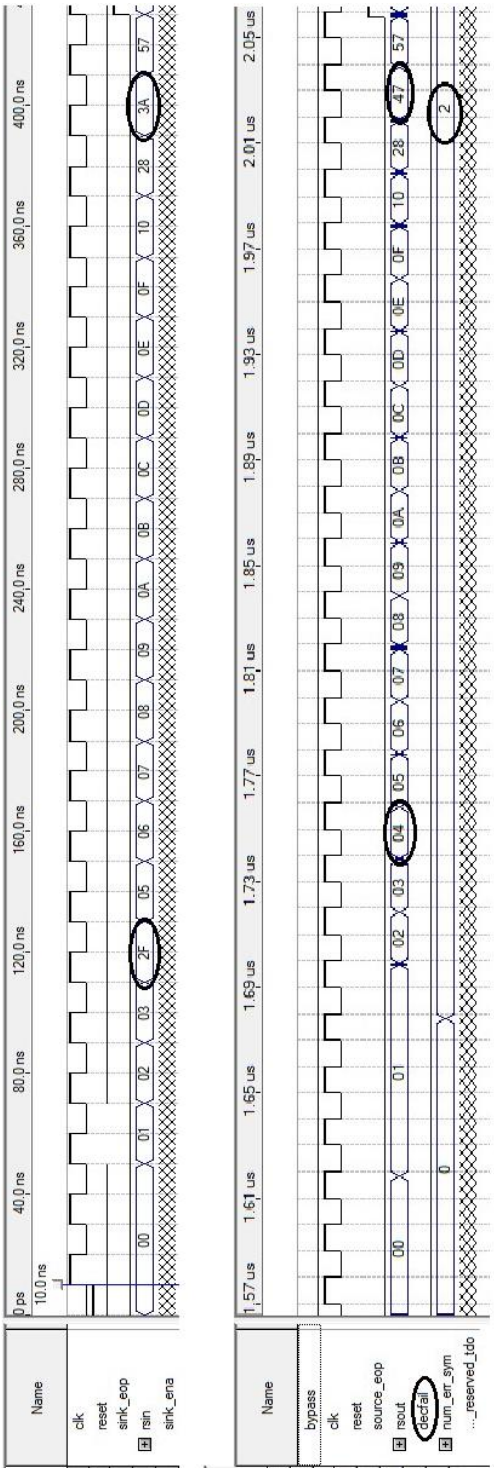


Fig. 1. Reed-Solomon Decoder [4].

C. Practical implementation of the Reed-Solomon decoder

A system of Reed-Solomon encoding and decoding was developed on bases of FPGA microchip. The encoder and decoder can be realized on the basis of a library module.



a) **b)**

Fig. 2. Sent encoded information (a) and its correction by the decoder (b).

Figure 2 (a) represents waveform simulation of operation of the device when introducing errors in two bytes of encoded word. Instead of the value 0x04 the value 0x2F is input to the decoder and instead of 0x47 – 0x3A.

Figure 2 (b) demonstrates that the decoder has restored the fourth data byte of and the second correction byte that came with errors. Value of line *num_err_sym* is "2", which corresponds to the existence of two defective bytes. The value on line *decfail* is equal to "0", which indicates that all errors were detected and corrected.

Adding to the 16 data bytes 4 correction bytes allows to detect and corrected any 2 bytes in the data packet. Therefore, in this case the Reed-Solomon decoder can recover the received data, if the number of errors does not exceed 1/10 of the total amount of data and all errors are accumulated in no more than two bytes.

IV. Implementation Of Wyner-Ash Decoder

A. Wyner-Ash codes

For implementation of the convolution coding and decoding the most optimal from the point of view of hardware resources is Wyner-Ash code. For our purposes a Wyner-Ash code with 8-bit codewords was chosen, of which 7 are informational bits and 1 – correction bit. In this case, to calculate a correction bit the current codeword is used and also 3 previous words. Thus, for the 4-th data word encoding is performed according to the following formulas:

c[1]=l1[7]^l1[6]^l1[5]^l1[4];

c[2]=l2[7]^l2[6]^l2[3]^l2[2]^c[1][m];

c[3]=l3[7]^l3[5]^l3[3]^l3[1]^c[2][m];

c[4]=l4[7]^l4[6]^l4[5]^l4[4]^l4[3]^l4[2]^l4[1]^c[3][m];

where l1, l2, l3 - previous codewords with c[i] – correction bits; c[4] - a check bit for l4-th word.

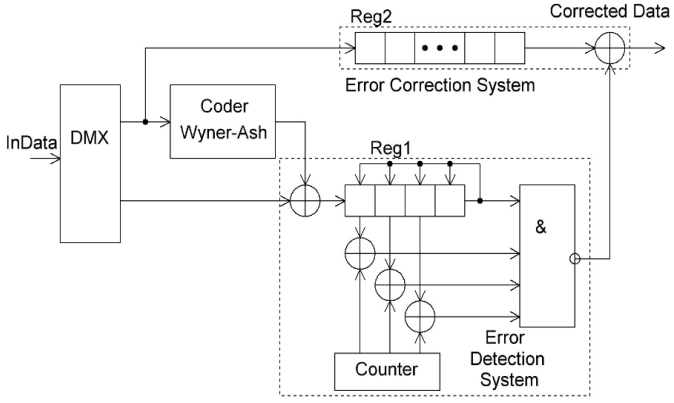


Fig. 3. Wyner-Ash Decoder [4].

The decoder scheme includes an encoder, an error detection and localizing system and error correction system (Fig. 3).

B. System of error detection and correction

In calculation of the syndrome, correction bits of the current codeword l4 are involved and of the following three – l5, l6, l7. At the same time, for calculation of these correction bits values of these data word are used and also of the previous three – l3, l2, l1.

The syndrome S is determined as a result of the comparison of four received correction bits with ones calculated using the formula:

S[i]=b[i]^br[i]; i=4,5,6,7;

br[4] – received correction bits of the current codeword;

br[5], br[6], br[7] – received correction bits of the following codewords;

b[4]-b[7] – calculated correction bits;

Formula (2) is used for the current codeword and for three following words. The first bit of the syndrome S[4] indicates presence of an error in the current l4 word. The position of the error is obtained in binary code by values S[5], S[6], S[7]:

Err_Pos = S[5]+S[6]*2+S[7]*4;

C. Practical implementation of Wyner-Ash decoder

Wyner-Ash decoder was implemented on a FPGA chip, which allows to accelerate the processing by carrying out calculations in the form of a conveyor. However, since the code is recursive, after an error was corrected it is necessary to stop the input data flow, to shift data on three positions backward and repeat calculation of the correction bits of the following codewords based on the corrected.

Algorithm of the decoding process is presented in fig. 4.

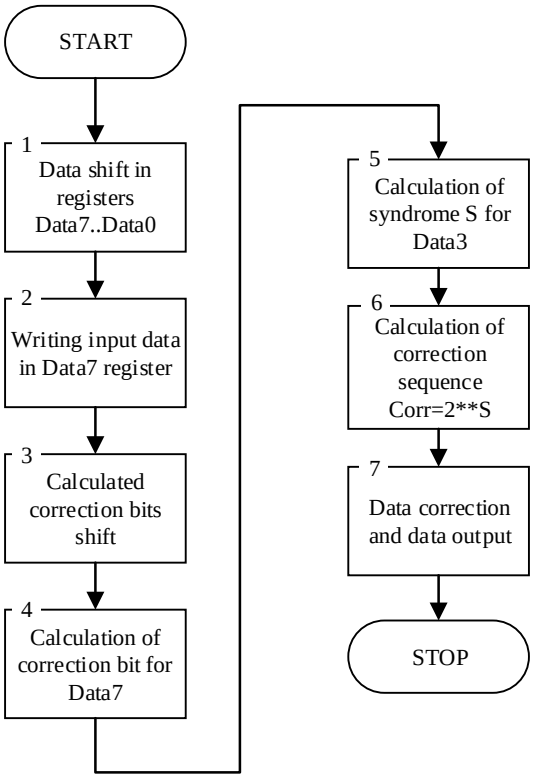


Fig. 4. Wyner-Ash Decoding process.

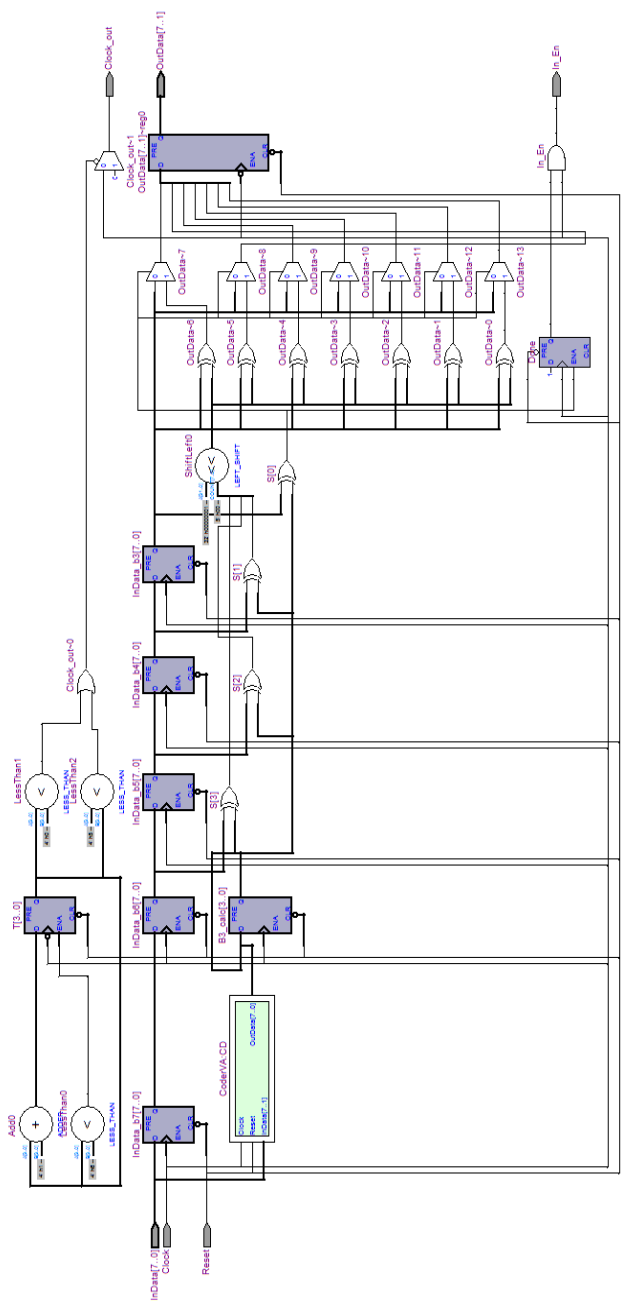


Fig. 5. RTL-diagram of Wyner-Ash Decoder.

Decoding system was implemented in design system Quartus II design using VHDL (Hardware Description Language). In the result an RTL-diagram was obtained presented in Fig. 5.

Waveform simulation of the decoding process is presented in Fig. 6. The diagram represents introduction of an error in in 3rd bit of the 4th codeword and its correction by the decoder. Therefore, in our case, the decoder can correct 1/8 of transmitted data if no more than one bit in one codeword is damaged.

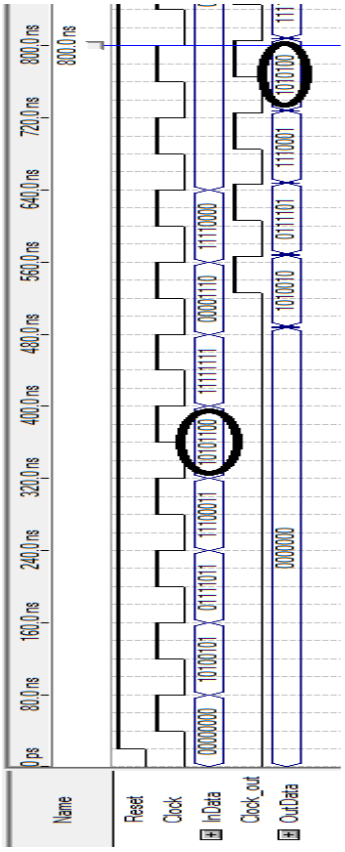


Fig. 6. Waveform simulation of Wyner-Ash decoding process.

V. Conclusion

Elaboration of error-correcting coding system requires taking into account its correcting ability and the types of errors that occur in the communication channel. However, realization of a decoding system is much more complex and processing of large amounts of video data requests to minimize hardware complexity, and speed of data processing. To make the decoding system able to correct different types of errors the concatenated coding was applied – a combination of convolutional (Wyner-Ash) and block (Reed-Solomon) coding. These codes along with high correcting ability have a comparatively low hardware complexity and implementation of described methods on FPGA allows to minimize processing time.

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