

Development of Conductive Nanotemplates on ZnSe

Eduard MONAICO¹, Ion TIGINYANU^{1,2}, Gleb COLIBABA³, D. D. NEDEOGLO³,
Ala COJOCARU⁴, Helmut FÖLL⁴

¹ National Center for Materials Study and Testing, Technical University of Moldova,
m_eduard_y@yahoo.com

² Laboratory of Nanotechnology, Institute of Electronic Engineering and Nanotechnology,
Academy of Sciences of Moldova, Chisinau 2028, Moldova
tiginyanu@yahoo.com

³ State University of Moldova, Chisinau 2009, Moldova
GKolibaba@yandex.ru, nedeoglo@usm.md

⁴ Chair for General Materials Science and Microwave Laboratory,
Christian-Albrechts-University of Kiel, Kaiserstr. 2, Kiel 24143, Germany
alaspri@yahoo.com, kb@tf.uni-kiel.de

Abstract – We demonstrate the possibility to fabricate arrays of pores oriented perpendicular and parallel to the top surface of the ZnSe nanotemplate. The control of material conductivity allows one to produce porous ZnSe samples with the mean pore diameter and characteristic skeleton wall thickness from several hundreds of nanometers to about 15 nm. In addition, electrochemical treatment of ZnSe single crystals using photoresist masks allows one to prepare buried porous structures with pores directed parallel to the top template surface, which is especially important for photonic applications.

Index Terms – electrochemical etching, porous ZnSe, in-plane approaches, wide-band-gap semiconductor nanotemplates, morphology characterization.

I. INTRODUCTION

Nanotemplates are widely used in nanofabrication, particularly in the production of large assemblies of nanowires and nanotubes of various materials with defined diameters and lengths. For many concrete applications it is necessary to integrate a large amount of nanowires in one bundle or array to achieve required functionalities. Over the last decade, different template-based nanofabrication approaches have been developed which offer the possibility to produce large assemblies of nanowires and nanotubes of various materials with defined diameters and lengths. Two types of templates are widely used for nanofabrication purposes, namely porous Al₂O₃ [1-4] and etched ion track membranes based either on inorganic materials or on organic polymers [5,6]. Both, porous Al₂O₃ and etched ion track membranes, however, exhibit high resistivity and therefore they often play a passive role in nanofabrication processes. In particular, templated growth of nanowires via electroplating is provided usually by the metal contact deposited on the back side of the high-resistivity membranes, while electroplating of metal nanotubes requires additional technological steps e.g. chemical modification of the inner surface of the pores prior to electrodeposition which leads to the incorporation of spurious phases in the nanotube walls. In this connection an important technological task is the development of cost-effective semiconductor nanotemplates which properties could be easily controlled by external illumination, applied electric fields etc. We have proposed a cost-effective technology for controlled fabrication of semiconductor nanotemplates with self-organized quasi-ordered distribution of nanochannels using anodic etching of III-V (GaAs, InP) and II-VI (CdSe)

crystalline substrates in a neutral electrolyte [7-9]. Besides, the feasibility of indium phosphide nanotemplates for electrochemical deposition of arrays of platinum nanotubes with diameters both larger and smaller than 100 nm was demonstrated [7].

The electronic band gaps of InP, GaAs and CdSe are 1.3; 1.4 and 1.7 eV at 300 K respectively, which means that the nanotemplates based on these materials are opaque in the visible region of the spectrum. Among III-V and II-VI semiconductors one may consider the wide band gap compounds GaN (E_g = 3.3 eV), ZnO (3.3 eV) and ZnSe (2.7 eV) as good candidates for the fabrication of conductive nanotemplates transparent in the visible region. We were forced to exclude the first two materials from consideration since GaN crystalline substrates are not yet commercially available, while ZnO, according to our preliminary studies, seems to be inappropriate for electrochemical pore growth. It is difficult to obtain wide bandgap semiconductors, like ZnSe, with high electrical conductivity due to self-compensation phenomena inherent to these materials [10].

In connection with this, over the last years special efforts have been undertaken at the State University of Moldova which resulted in the development of an approach of co-doping ZnSe by Al and Zn impurities for the purpose of controlling the material electrical conductivity necessary for the application of the technology of electrochemical porosification [11].

II. PREPARATION OF ZnSE NANOTEMPLATES

We used 1 mm thick n-ZnSe substrates with free electron concentrations from $7 \times 10^{16} \text{ cm}^{-3}$ to $2 \times 10^{18} \text{ cm}^{-3}$. A method based on doping the samples with Al from a Zn+Al melt was used for controlling the conductivity of ZnSe

crystals [11]. This doping procedure allows one to produce suitable conductive samples for controlled nanostructuring using electrochemical etching techniques.

Anodic etching of ZnSe was carried out in dark at room temperature in $K_2Cr_2O_7:H_2SO_4:H_2O$ electrolyte with the ratio 5:100:10. Anodization was performed in potentiostatic regime in an electrochemical double cell as described elsewhere [12], the sample being mounted between the cells. The area of the sample exposed to the electrolyte was 0.25 cm^2 . The electrolyte was pumped through both cells in a continuous mode. A four-electrode configuration was used [12]: a Pt reference electrode in the electrolyte, a Pt sense electrode on the sample, a Pt counter electrode, and a Pt working electrode. The electrodes were connected to a specially designed potentiostat. The applied voltage was varied from +5 V to +30 V for ZnSe samples, depending on the substrate conductivity. After growth of pores, the top nucleation layer of samples was removed by isotropic wet etching.

A TESCAN Scanning Electron Microscope (SEM) equipped with an Oxford Instruments INCA Energy Dispersive X-ray (EDX) system was used to study the morphology and chemical composition of the samples.

III. MORPHOLOGY CHARACTERIZATION OF ZNSE NANOTEMPLATES

The anodization of ZnSe substrates with electron concentration of $7 \times 10^{16}\text{ cm}^{-3}$ at the applied voltage of 25 V results in the formation of pores with the mean diameter of around 400 nm (Fig. 1a), while pores with the mean diameter of around 40 nm are produced in ZnSe substrates with the electron concentration of $2 \times 10^{18}\text{ cm}^{-3}$ anodized at 8 V (Fig. 1b). The width of the porous skeleton walls correlates with the diameter of pores, i.e. in all porous samples the width of the skeleton walls proves to be nearly equal to the pore diameter. Note, that the minimum pore diameter obtained by electrochemical etching of ZnSe until now is 40 nm [13]. According to our explorations, the higher is the electron concentration, the lower should be the applied voltage during anodization, and the smaller is the diameter of the pores produced. We succeeded to reduce the pore diameter down to 15 nm by anodization of ZnSe substrates with the electron concentration of $2 \times 10^{18}\text{ cm}^{-3}$ at 5 V, but the porous skeleton walls thickness in this case remain around 40 nm. This can be explained by overlapping in the pore wall of two regions representing depletion layers. Thus, to reduce the wall thickness is necessary to further increase the electron concentration in ZnSe substrates, which unfortunately cannot be easily realized. But, for some applications of nanotemplates it is not strictly necessary to have small pore wall thickness. Due to reduction of pore wall thickness the number of free electron concentration is also reduced. At the same time it is clear that for uniform electrochemical deposition of metal species on the inner surface of pores along the whole length, the semiconductor nanotemplates have to possess high skeleton conductivity.

We explained for the first time the dynamics of pore growth in n-ZnSe by analyzing the development of the pore morphology as a function of depth and demonstrated the

possibility to use a porous ZnSe matrix for the purpose of electroplating arrays of metal nanotubes [14].

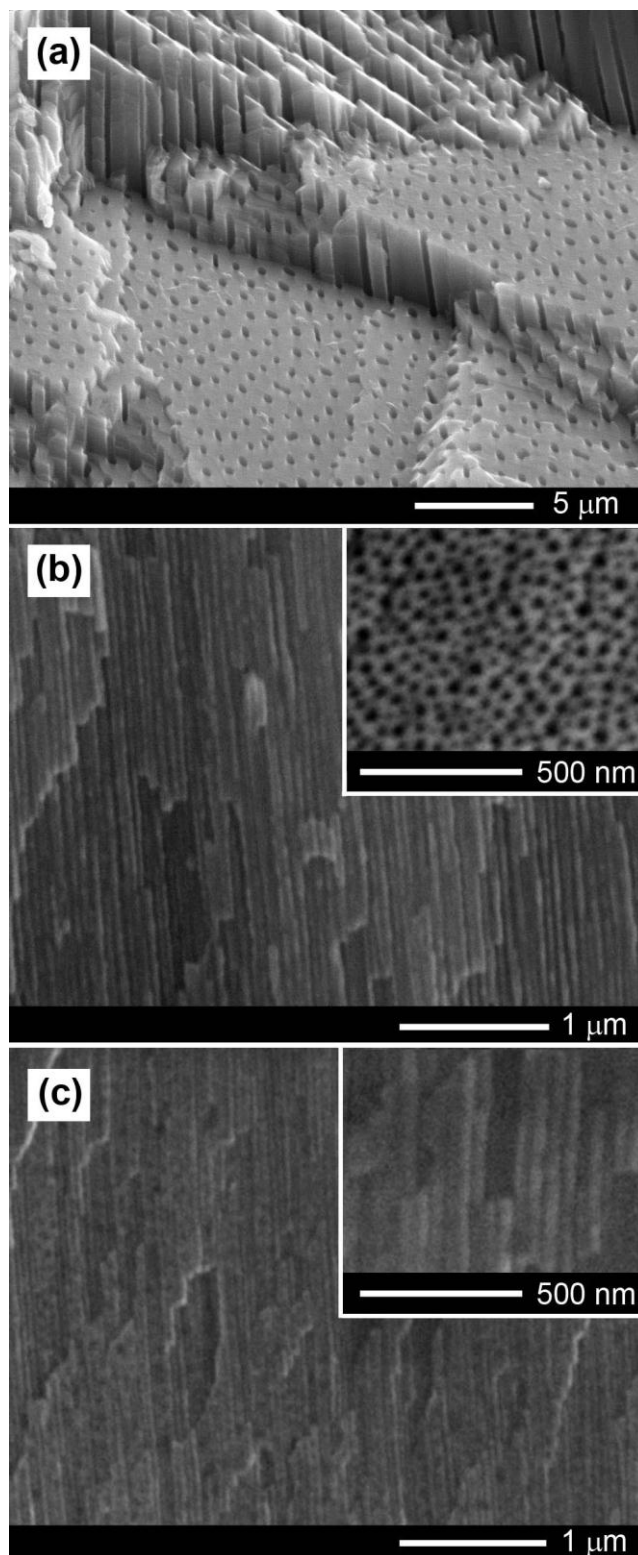


Fig. 1. SEM images taken from ZnSe nanotemplate prepared on crystalline substrates with free electron concentration of $8 \times 10^{16}\text{ cm}^{-3}$ (a) and $2 \times 10^{18}\text{ cm}^{-3}$ (b,c) by anodization in a $K_2Cr_2O_7:H_2SO_4:H_2O$ electrolyte with the ratio of 5:100:10.

The possibility to control the diameter of pores just by changing the applied potential during anodic etching enables one to prepare multilayer porous structures in one technological process. Thus, successive anodization of ZnSe

substrates at varied applied voltage results in layer porosification at different length scales [14].

IV. IN-PLANE TECHNOLOGICAL APPROACHES OF ZNSE NANOTEMPLATE FABRICATION

Porous ZnSe structures with pores propagating in the direction parallel to the sample surface (Fig. 2a) are of especial interest for the fabrication of two-dimensional photonic crystals, including metallo-dielectric ones, since this geometry allows a wide implementation of structures which can be easily explored under different polarizations of the incident electromagnetic radiation.

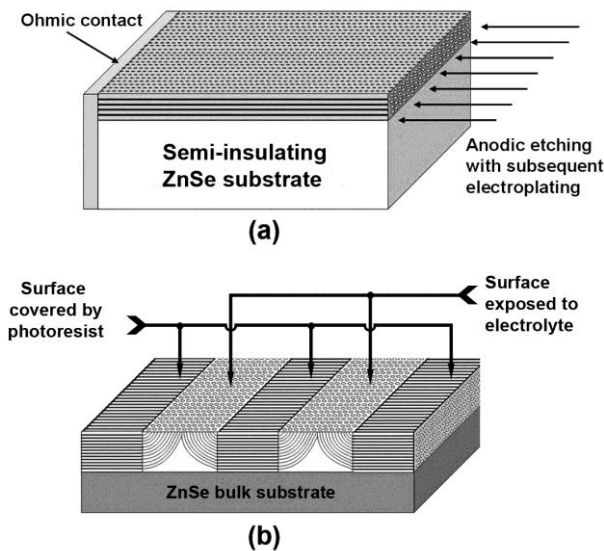


Fig. 2. (a) Schematic representation of the technology for the preparation of nanotemplates with pores propagating in the direction parallel to the sample surface (in-plane approach) and (b) after optimization of the etching conditions.

Nanowires and nanotubes are generally grown in the perpendicular direction to the substrate surface. Nanowires grown in-plane with the substrate surface are more suitable for conventional planar processing techniques. The first approach was initially demonstrated using GaAs [15], but in-plane growth from etched facets (such as sidewalls and V-grooves) on the substrate surface has been more widely used for Si [16-18]. On the Si (110) substrate, deep trenches with (111) side walls can be easily formed by anisotropic etching.

While the design shown in Fig. 2a is more suitable for in-plane porosification of epilayers, the approach shown in Fig. 2b proves to be efficient for in-plane pore growth in bulk substrates. In the latter case the ohmic contact is deposited onto the opposite surface of the sample, and electrochemical etching is performed through windows in the photoresist. The experiments demonstrated that the electrochemical etching starts at the interface between the open surface and the electrolyte. Consequently, due to the high conductivity of the sample, the pores propagate along the current lines in all directions, inclusively underneath the photoresist in a direction parallel to the sample surface, as illustrated in Fig. 3. Moreover, the photoresist can be easily dissolved in base solution.

An interesting feature of porous structures obtained by this method is the fabrication of buried porous layers, as illustrated in Fig. 3. The pores grow under a thin surface

layer which remains intact during the electrochemical treatment. The thickness of this surface layer is of the order of the surface depletion region, i. e. from several tens to several hundreds of nanometers, depending on the conductivity of the anodized substrate. A three layer structure is shown in Fig. 8a for a ZnSe sample, where a resist layer is reminiscent on a part of the sample. A surface layer of the virgin ZnSe is seen under the resist layer, and the porous structure is buried under this surface layer.

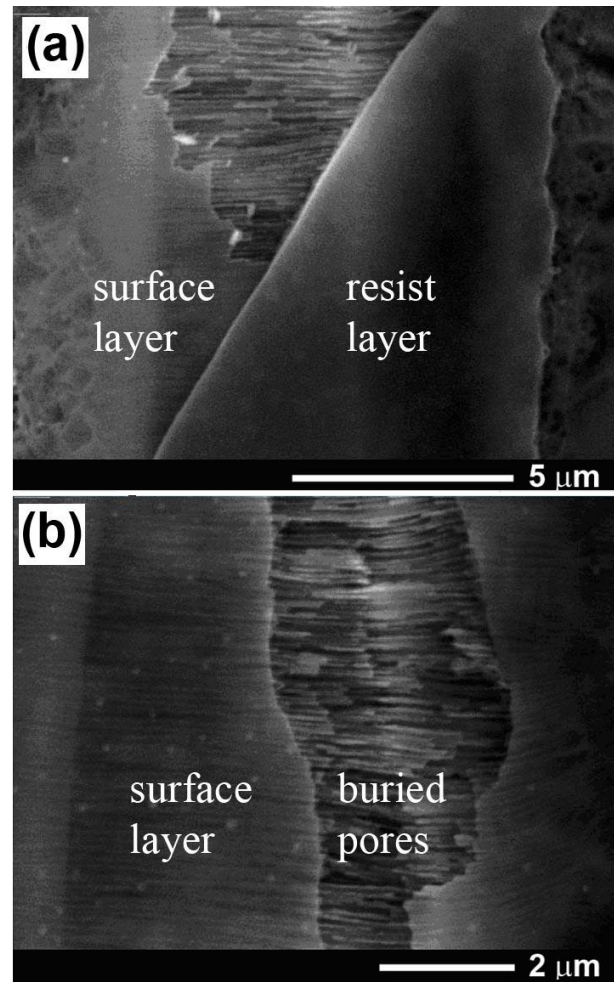


Fig. 3. Porous structures buried in ZnSe substrates.

The developed ZnSe nanotemplates with pores parallel to the crystal surface are suitable for the electrochemical deposition of metals inside pores, similar to the nanotemplates with pores perpendicular to the surface of the sample.

V. CONCLUSION

The results of this study demonstrate the possibility to fabricate porous ZnSe nanotemplates with uniform distribution of pores and geometrical parameters controlled by the conductivity of the substrate and the technological conditions applied by etching in a $K_2Cr_2O_7:H_2SO_4:H_2O$ electrolyte. Electrochemical treatment in these electrolytes using photoresist masks allows one to prepare buried porous structures with pores directed parallel to the template top surface, which is especially important for photonic applications.

The high conductivity of the semiconductor nanotemplate skeleton provides conditions for uniform electrochemical deposition of metal species on the inner surface of pores. Moreover, the high value of the refractive index of ZnSe and its transparency in the visible region suggest that metallo–semiconductor structures are promising for the elaboration of negative refractive index metamaterials, in particular of novel focusing elements and beam splitters for applications in the visible region of the spectrum.

ACKNOWLEDGMENTS

This work was supported by the Supreme Council for Research and Technological Development of the Academy of Sciences of Moldova under grant no 11.819.05.12A and by Alexander von Humboldt Foundation.

REFERENCES

- [1] M. V. Kamalakar and A. Raychaudhuri, A Novel Method of Synthesis of Dense Arrays of Aligned Single Crystalline Copper Nanotubes Using Electrodeposition in the Presence of a Rotating Electric Field. *Advanced Materials*, vol. 20, pp. 149–154, 2008.
- [2] Y. Piao, H. Kim, Fabrication of nanostructured materials using porous alumina template and their applications for sensing and electrocatalysis. *J. Nanosci. Nanotechnol.*, vol. 9, pp. 2215–2233, 2009.
- [3] S. Gaurav, M. V. Pishko and G. A. Craig, Fabrication of metallic nanowire arrays by electrodeposition into nanoporous alumina membranes: effect of barrier layer. *Journal of Materials Science*, vol. 42, pp. 4738–4744, 2007.
- [4] A. Ghahremaninezhad and A. Dolati, A study on electrochemical growth behavior of the Co–Ni alloy nanowires in anodic aluminum oxide template. *Journal of Alloys and Compounds*, vol. 480, pp. 275–278, 2009.
- [5] T.W. Cornelius, B. Schiedt, D. Severin, G. Pépy, M. Toulemonde, P.Y. Apel, P. Boesecke and C. Trautmann. Nanopore4s in track-etched polymer membranes characterized by small-angle x-ray scattering. *Nanotechnology*, vol. 21, 155702, 2010.
- [6] J. Duan, J. Liu, D. Mo, H. Yao, K. Maaz, Y. Chen, Y. Sun et al., Controlled crystallinity and crystallographic orientation of Cu nanowires fabricated in ion-track templates. *Nanotechnology*, vol. 21, 365605, 2010.
- [7] Ion Tiginyanu, Elena Monaico, Eduard Monaico, Ordered arrays of metal nanotubes in semiconductor envelope. *Electrochem. Commun.*, vol. 10, pp. 731–734, 2008.
- [8] I.M. Tiginyanu, V.V. Ursaki, E. Monaico, E. Foca, H. Föll, Pore Etching in III-V and II-VI Semiconductor Compounds in Neutral Electrolyte. *Electrochemical and Solid-State Letters*, vol. 10, D127, 2007.
- [9] I.M. Tiginyanu, E. Monaico, S. Albu and V.V. Ursaki, Environmentally friendly approach for nonlithographic nanostructuring of materials. *Physica Status Solidi (RRL)*, vol. 1, pp. 98–100, 2007.
- [10] Y. Marfaing, Self-Compensation in II-VI Compounds. *Prog. Cryst. Growth Charact.*, vol. 4, pp. 317–343, 1981.
- [11] G. N. Ivanova, D. D. Nedeoglo, N. D. Negeoglo, V. P. Sirkeli, I. M. Tiginyanu and V. V. Ursaki, Interaction of intrinsic defects with impurities in Al doped ZnSe single crystals. *J. Appl. Phys.*, vol. 101, 063543, 2007.
- [12] S. Langa, J. Carstensen, M. Christophersen, H. Foll and I. M. Tiginyanu, Observation of crossing pores in anodically-etched n-GaAs. *J Appl. Phys. Lett.*, vol. 78 pp. 1074–1076, 2001.
- [13] E. Monaico, I. M. Tiginyanu, V.V. Ursaki, A. Sarua, M. Kuball, D.D. Nedeoglo and V.P. Sirkeli, Photoluminescence and vibrational properties of nanostructured ZnSe templates. *Semicond. Sci. Technol.*, vol. 22, pp. 1115–1121, 2007.
- [14] E. Monaico, P. Tighineanu, S. Langa, H. L. Hartnagel and I. M. Tiginyanu ZnSe-based conductive nanotemplates for nanofabrication. *Phys. Stat. Sol. (RRL)*, vol. 3, pp. 97–99, 2009.
- [15] K. Haraguchi, K. Hiruma, K. Hosomi, M. Shirai and T. Katsuyama, Growth mechanism of planar-type GaAs nanowhiskers. *J. Vac. Sci. Technol. B*, vol. 15, pp. 1685–1687, 1997.
- [16] R. He, D. Gao, R. Fan, A. I. Hochbaum, C. Carraro, R. Maboudian and P. Yang, Si nanowires bridges in microtrenches: integration of growth into device fabrication. *Adv. Mater.*, vol. 17, pp. 2098–2102, 2005.
- [17] M. S. Islam, S. Sharma, T. I. Kamins and R. S. Williams, A novel interconnection technique for manufacturing nanowires devices. *Appl. Phys. A*, vol. 80, pp. 1133–1140, 2005.
- [18] M. S. Islam, S. Sharma, T. I. Kamins and R. S. Williams, Ultrahigh-density silicon nanobridges formed between two vertical silicon surfaces. *Nanotechnology*, vol. 15, L5–L8, 2004.