Structural aspects in the design for testability

"You will never solve a problem if you will think the same way as those who created it."
Albert Einstein

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Abstract -- Means of modern technology is the result of research and also constitutes an essential support in deepening research performance: no electronic microscopes, telescopes, without computers and lasers can be designed current scientific developments. Nontraditional approaches, and risk of major problems oldest and innovative results obtained at the frontiers of knowledge inspires hope in winning a very important scientific bastion: solving riddles logic synthesis aspects of primary structures in the micrometer and nanometer ranges. The transition to a new stage of knowledge involves not only the establishment of principles and original concepts. Equally important is the highlight and preserve the essential elements of the current state of scientific knowledge as a continuous development. The article contains an analysis of the current state of problem solving design for testability. Structural aspects are analyzed represent obstacles to solving the problem addressed (redundancy, fan-outs or similar opposite parity signal propagation to logic gate entrances convergence of structural design digital artifacts). Also are highlighted and analyzed a number of structural issues favorable to solve the problem (homogeneity, repetivitatea and regularity). Research into structural, functional and logic is of paramount importance in solving the problem of design for testability of digital structures.

***Index Terms* — desgn for testability, structural aspects, digital structures, fan out, homogeneity, test generation.**

I. INTRODUCTION

Design for testability (DFT) issue digital structures (DS) occurred in mid 60s of the twentieth century: the rapid development of integrated circuits (IC) and production based on their electronic microscopes and telescopes performant, serial production of the IBM 360 etc. fortified essentially scientific research potential and to obtain new results However, permanent increase functionality requirements but lead to complex structural-functional-logic them difficult or impossible to generate tests were timely. (See: [1] Bennetts: ″In fact the only real measure of testability is the cost of generating the corresponding set of tests for the circuit″ - pag. 53; [2] G. Russell, I.L. Sayers: ″ Results have shown that test generation times increase as the square of circuit complexity, assuming that a path sensitization algorithm is used and that the amount of backtracking to resolve inconsistencies is negligible″ - pag. 15-16).

As a result in diagnostic technique was a new scientific direction - design for testability, the main objective of which was to develop rules, concepts and principles of synthesis of easily testable DS. DS consist of two types of structures: combinational circuits (CC) and sequential circuits (SC). SC consists of CC and memory elements (ME). Generating tests for SC is a problem for many more complicated due to the presence of ME whose states must be known to generate tests. Testing a circuit is an experiment in which it is applied test inputs; ie primary input vector signal stimulants, selected according to certain requirements, and those reactions are observed outputs standard DS and compared with signals obtained in the test generation process. With the increasing complexity of DS manual test generation process has become very expensive and practically impossible. At the time of this impasse output were proposed two ways:

1 The development of efficient algorithms and, based on their respective programs generating tests;
2 Design for testability of DS.

To solve the first problem J.P. Roth [3] developed the test generation algorithm DALG I based on single path sensitization in DS. P. R Schneider [4] presented a digital structure, the so-called counterexample Schneider, for which, according to the author, the test for a given fault could not be developed, although there could be obtained by another method. As a result, Roth and Schneider have developed a new version of the algorithm - DALG II. [5], based on simultaneous awareness of all the ways outului fan site to logic gate (LG) inputs convergence. This variation of the algorithm D is very efficient and can be used to generate multi-level test logic DS, but with the condition that DS is developed in accordance with certain design principles. For DS, designed ad hoc or artifacts, such as the DS of [4], the tests can not be generated. In [6] it was shown that a counterexample DS Schneider is an ad-hoc structure with multiple redundancies and fan outs converging with different parities.

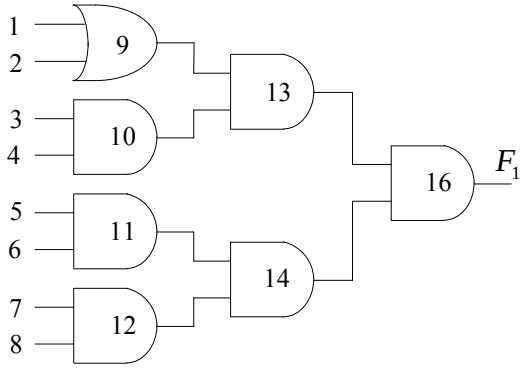

Figure. 1. Incomplet degenerate structure

Table 1. Tests for check of structure F_1

Nr.	Tests									Type of detected errors
	Primary inputs								Out-put	
	1	2	3	4	5	6	7	8	9	
1	0	0	1	1	1	1	1	1	0	1≡1, 2≡1
2	0	1	1	1	1	1	1	1	1	(2÷9) ≡0
3	1	0	1	1	1	1	1	1	1	1≡0, (3÷9) ≡0
4	1	0	0	1	1	1	1	1	0	3≡1
5	1	0	1	0	1	1	1	1	0	4≡1
6	1	0	1	1	0	1	1	1	0	5≡1
7	0	1	1	1	1	0	1	1	0	6≡1
8	0	1	1	1	1	1	0	1	0	7≡1
9	0	1	1	1	1	1	1	0	0	8≡1

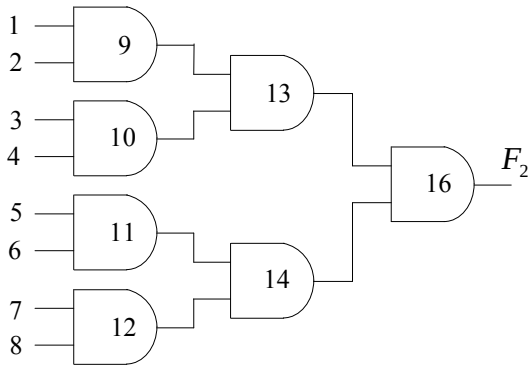

Figure 2. Maximal degenerate structure

Table 2. Tests for check of maximal degenerate structure F_2

Nr.	Tests									Type of detected errors
	Primary inputs								Out-put	
	1	2	3	4	5	6	7	8	9	
1	1	1	1	1	1	1	1	1	1	(1÷9) ≡0
2	0	1	1	1	1	1	1	1	0	1≡1,
3	1	0	1	1	1	1	1	1	0	2≡1
4	1	1	0	1	1	1	1	1	0	3≡1
5	1	1	1	0	1	1	1	1	0	4≡1
6	1	1	1	1	0	1	1	1	0	5≡1
7	1	1	1	1	1	0	1	1	0	6≡1
8	1	1	1	1	1	1	0	1	0	7≡1
9	1	1	1	1	1	1	1	0	0	8≡1

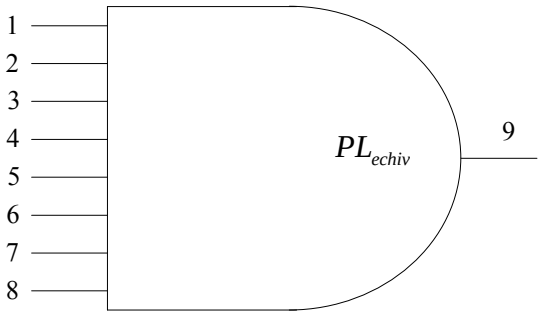

Figure 3. Echivalent logic gate

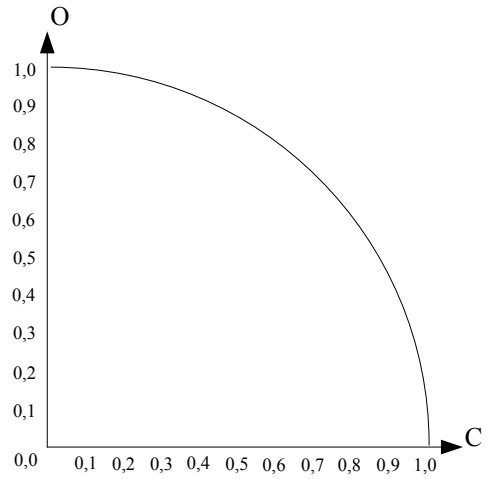

Figure 4. Dependence homogeneity/complexity

Moreover, the connection itself, whose fault is considered detectable in [4] by using DALG II, is redundant, representing output connection of logic gates as redundant. It follows two conclusions: connection, whose fault is considered detectable in [4] by using DALG II, is redundant, representing output connection of logic gates as redundant. It follows two conclusions:

1 Any effective would be a test generation algorithm, it can not overcome the artifacts of inadequate or ad hoc designed DS;

2 Comparison of efficiency DALG I and DALG II is not appropriate:

DALG I algorithm involves the activation of a single way thtough circuit fan out site to the respective inputs of LG convergence and leads to the generation of fault location tests, when the algorithm DALG II is based on the simultaneous activation of all pathways through circuit fan out site to the respective inputs of LG convergence and leads to the generation of fault detection tests [7]. Detection and fault location are two distinct processes, efficiency and rezultativitatea which can not be compared.

II. STRUCTURAL ISSUES IN DESIGNING FOR TESTABILITY

After half a century of putting PPT problem, it was solved just enough SC to the current state of knowledge. Although initially found to solve the problem of SC DFT will be much more difficult than solving the problem of CC DFT, this was not true. Contrary to expectations, solving the problem for CS PPT advanced considerably in comparison with the state to resolve the problem PPT for CC. SC consists of CC and ME. In principle, ME structures (registers, adders, counters) carried out largely static until operations, receipt, storage, processing logic, and / or transmitting information. However, the dynamic operation of a SC is the logic combinaționlă, ie CC. Without the proper disposal of DFT CC is impossible and the proper disposal of DFT to SC.

It should be noted that both Schneider counterexample and other results "negative" were natural steps in the scientific research and not scientific falsification. Rather it can be said that the problem DFT was made too early, at that stage of knowledge at the time of being insufficient to solve the problem: structural, functional and logical DS, and the principles and concepts of DFT were unknown or incipient.DFT appropriate design principles and concepts tested were developed CC. However, neither the current state of knowledge is not enough to solve the problem of CC DFT. Urgent need to address this issue is essential for the synthesis of micrometer and nanometer level DS. Research aspectrelor structural, functional and logical primary cells can lead to new results in solving the problem of DFT.

II.1. The objectives of the analysis and synthesis

The analysis and synthesis are the two complementary sides of one and the same entity: analyzing the structure of research aimed at obtaining structural aspects of the truth table and / or logic function (LF) produced by the structure under consideration, in the synthesis of a logical structure based on functional aspects, ie the truth table (TT) that logical function that adequately describe the LF to be achieved.So look structural and functional aspect of representation are two phases of the same entity. Logical aspects of the representation of the structure in the range micrometric and nanometric are a first step towards the next stage of knowledge and problem solving DFT to DS.

II.2. Structural aspects and problems of DS

Algebraic systems are called crowds, in addition to binary operations are defined and certain relationships. Algebras are particular cases of algebraic systems, the set of relations which is empty. Algebra consisting of the set ordered with all possible binary operations, called algebra of logic. Algebra consisting of the ordered set M_n and binary opeation disjunction □, conjunction & and negation in M_n is called Boolean algebra. A structure is an algebraic system $\{ M_n ; \leq; \cap, \cup \}$ consisting of the ordered set of binary vectors of *n* rank ordered, a binary relation (≤) and two binary operations - the conjunction ∩ and disjunction ∪ .

Structure in the general case, reflects the level of organization of matter. Instantiation of the concept of DS is the interaction with the outside elements (primary inputs), some internal ordering and interdependence between logic gates (LG), which provides DS operation result output connections observed [7, 8].

In terms of the number of entries of LG is connected to an output of a previous LG the DS can be classified into three groups:

1). DS without fan outs;

2). DS fan connections outs only primary inputs (PI);

3) DS with fan outs both PI connections, as well as internal connections. The presence of fan outs internal connections are potential sources of imposibiltății generation tests. Namely internal organization, ordering and interdependence LG lead to the occurrence of the DFT. For example, the artifacts methods to minimize and synthesis can lead to the obtaining of non tested DS. Fan outs with opposite parity signal propagation paths to convergence LG entrances leading to inability to obtain homogeneous sets (00...0 or 11 ... 1) and, hence, to the impossibility of detecting errors OR LG ≡ 1 and errors ≡ 0 for LG and DALG II algorithm.. Similarly, fan outs with similar parity signal propagation paths to convergence LG entrances leading to inability to obtain nonhomogeneous sets (100...0 or 011...1 or 0 ... 1) and, hence, to the impossibility of detecting errors ≡ 0 for LG OR and errors ≡ 1 for LG AND in algorithm DALG II. The connection previous fan out is just an artifact - in this case it represents an entity belonging simultan to multiple LG. Or, this phenomenon contradicts the way of representing essential implicanțelor minimal form of LF Moreover, essen□ial implicants fall in each of the forms of minimal representation of LF and theit modification constitutes an artifact. DS redundancy aspect is a structural loops, which can prevent the generation of the test detection / localization of specific defects or defects may be due to masking. These difficulties of the DFT in the current state of knowledge hampers addressing DFT.

II.3. Favorable structural aspects address the DFT

II3.1. DS homogeneity

The transition to a new state of knowledge does not imply destruction or neglect of previous knowledge. Had held important knowledge of principles and concepts do not contradict the current state of knowledge and can be the part of the foundation of the new state of knowledge. Experience, or even failed to address the DFT has its positive moments obtained in the search of solutions DFT problem. Practice test generation indicates that certain properties DS tests can be obtained easily. Moreover, some configurations DS enabling the test practically directly without generating tests as such. DS homogeneity are a structurally well.

We consider the DS in Figure 1. Numbers 1 ÷ 8 are assigned to LG (and their output connections). DS of figure 1 is composed of LG and just being the type or LG 9. Such structures are called incomplete degenerate DS. Tests for these DS are obtained easily, as can be seen from Table 1. Even simpler to obtain maximal degenerate DS tests for figure 2: DS determines univocally the structure and number of tests. SD maximal degenerate (figure 2) is equivalent to the logical AND gate in figure 3. In other words, a degenerate maximum DS is a homogeneous structure, consisting of one type of LG (OR or AND), equivalent to a single LG (OR or AND). Hence the four properties as amazing as it is useful:

1 LG type and number of primary inputs uniquely determines the structure of the tests and their number is not needed to generate test procedure;
2 set of tests contains a minimal number of tests;
3 set of tests so obtained detects all possible single errors such ≡ ≡ 0 and type 1 connections LG equivalent;
4 The set of tests of error detection is test set of error localization LG [10 These results are crucial in addressing DFT. Note that it is necessary to refer to the relationship between homogeneity and complexity of logic functions (figure3). Possible achievable: homogeneous structures realized one primary LF. It follows that research is needed to find solutions to bypass this obstacle, now impassable.

II.3.2. DS repetitive and / or ordered

In the design DS fragments can be obtained with the same circuit structure. In this case a fragment generated tests can be used in the synthesis process of a set of tests for the entire circuit, lowering the costs of generating tests. Also in this context, to DS may contain fragments arranged in a certain way, which may also facilitate the generation of tests. Using DS repetitive and / or sequenced in the PPT is preferable because it can lead to minimizing costs related to generating tests.

III. CONCLUSIONS AND FUTURE RESEARCH

Work is a first step to address the design for testability approach to DS in the range of micrometers and nanometers. Research into structural, functional and logic is to:

1. Highlighting artefacts digital structures that occur throughout the design process, from checking DS and ending with exclusion logic redundancy;2. Check logic functions minimality and accuracy of the results obtained at each stage;
3. Avoiding fan outs;
4 Use, where possible, homogeneous structures, repetitive and / or ordered;
5. Research and seeking new innovative solutions to the problem of analysis of primary structures of biological cells in order to obtain appropriate logical descriptions.
6. Development of new innovative concepts to solve the problem PPT beyond the current state of knowledge.

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