Nano Metrology Aspects of Design, Simulation, Fabrication, Testing , Reliability and Failure Analysis of Wafer Fused VCSEL

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***Abstract* – In this paper are presented several application aspects of nano metrology tools in characterization and fabrication of high performance long wavelength wafer fused VCSELs as well as for failure analysis. As long wavelength VCSELs are emerging as attractive light-sources for replacing DFB lasers in power consumption sensitive applications, the main challenges in developing the cost and time efficient nano metrology tools for supporting processing and characterization are discussed.**

***Index Terms* – Long-wavelength, VCSELs, wafer fusion, VCSEL technology, failure analysis, nanometrology**

I. INTRODUCTION

Long wavelength (LW) vertical cavity surface emitting lasers (VCSELs) emitting in the 1300 and 1550 nm band with single mode (SM) output power in excess of 1mW in a wide temperature range up to 85°C, high speed modulation capabilities and accurate emission wavelength setting present interest in broad band optical communications, and sensing . Compared with standard distributed feedback (DFB) edge-emitting lasers, VCSELs offer advantages of

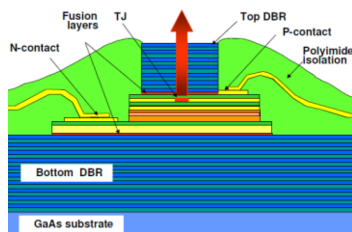


Fig. 1. Schematic cross section of the wafer fused 1310 nm VCSEL

symmetric far-field emission pattern, low power consumption and continuous wavelength tuning with current. State of the art longwavelength VCSELs with increased single mode output power have a hybrid structure combining GaAs/AlGaAs or dielectric distributed Bragg reflectors (DBRs) for high reflectivity with InP/InAlGaAs quantum well (QW) active regions for high optical gain at elevated temperatures. In addition, employing tunnel junctions has allowed intra-cavity contacting with low-absorption DBRs, a crucial ingredient for reaching high single mode power and high modulation speed. Among all leading LW-VCSEL technologies, localized wafer fusion offers the greatest flexibility in selecting the emission wavelength while the utilized GaAs/AlGaAs DBRs provide the best thermal conductivity . Consequently, the wafer fusion approach yielded 1300 and 1500 nm VCSELs with state of the art performances [1,2]. In this paper we describe the design, fabrication process and characterization results of wafer fused 1310 and 1550 nm single-mode VCSELs with lower power consumption as compared with corresponding DFB edge-emitting lasers at the same output power level of 1mW and operation speed above 5 Gb/s . The capability of cavity adjustment for setting the emission wavelength in a specified position of the CWDM grid, on the full wafer-scale industrial fabrication process demonstrates the possibility of wavelength inventory selection in the range 40 nm on the same 2-inch VCSEL wafer. The first documented reliability data obtained on wafer-fused VCSELs processed in the industrial wafer fab of a leading optical component manufacturer in Europe. Results show that VCSELs fabricated with the wafer-fusion technique and displaying high performance level, meet Telcordia generic requirement standards. Finally, the first results of implementing state of the art nanometrology tools for failure analysis as well as the main challenges in decreasing the cost and duration of full range on ongoing failure analysis are briefly discussed.

II. VCSEL DESIGN AND SIMULATIONS

The VCSEL device structure comprises an InP-based 5/2 λ-active cavity that is fused on both sides to undoped AlGaAs/GaAs DBRs, as schematically depicted on Figure 1. The active cavity includes an InAlGaAs/InP multi-QW region with 4-6 compressively strained quantum wells and a p++/n++ InAlGaAs tunnel junction."

Figure 2 presents transverse gain and mode profiles of this design at different temperatures that were obtained by numerical solving of a fully coupled 2-dimentionsional set of elctro-opto-thermal equations [4].

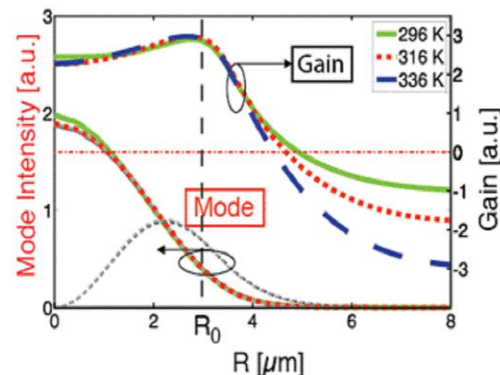


Fig. 2. Lateral gain and optical field distributions from the center of the tunnel junction . Ro represent the edge of a TJ mesa with diameter of 6 um

As one can observe the fundamental mode is predominant and the gain and mode profiles spread by about 1-1.5 µm outside the active region defined by the tunnel junction mesa. The optical confinement is due to a lateral refractive index variation that corresponds to a difference in the optical

paths of about 7 nm for the light propagating through the tunnel junction mesa and adjacent re-grown InP.

III. FABRICATION AND TESTING

The InP-based active cavity and GaAs-based DBRs are grown by low pressure metal-organic vapor phase deposition (LP-MOVPE) on 2 (100) wafers [3] . A mesa-structure of 6-7 µm in diameter formed in the tunnel junction that is regrown with n-type InP serves for carrier and photon confinement.

Electrical contacting is performed by top and bottom intra-cavity n-InP layers. This contacting scheme allows using un-doped top and bottom DBR mirrors. InGaAsP cavity adjustment layers that are located on both sides of the active cavity serve for precise adjustment of the emission wavelength.

Figure 4 depicts images of tunnel junction mesas at different stages of the fabrication process: a- initial mesas etched in the tunnel junction, b,c after regrowth, before first fusion step, d, e-after the first fusion step. As one can observe from Figure 4, after re-growth mesas have elliptical shape and a size that is 2-2.5 times larger compared with initial mesas that have a round shape (please note that the image size and picture resolution are not enough to give all the details, Figure 4 should be considered only for concept description). This occurs due to predominant lateral overgrowth with a tendency to planarization occurring during regrowth by MOVPE. Consequently, the optical mode, that extends by about 1.5 µm outside the active region defined by the mesa etched in the tunnel junction (Figure 4) is well within the edges of the re-grown region that will help in selection of the fundamental mode. The elliptical shape of the regrown mesa provides a way for discrimination of polarization modes. Before the first fusion process, the top InGaAsP cavity-adjustment layer is selectively etched on one half of the wafer. The oblique line on Figure.2,c represents the border between two regions on the wafer with different cavity lengths.

During the fusion process, InP-based and GaAs-based 2-inch wafers are brought into contact at 600°C in vacuum, and by applying a pressure of 7000 N for 30 min in an industrial custom-built wafer bonding machine. At these values of temperature and pressure, both wafers undergo a slight plastic deformation resulting in a uniform contacting on a nanometer scale. As a result, covalent bonds are formed between InP-based and GaAs-based wafers. After cooling down the stack that includes InAlGaAs/InP-AlGaAs/GaAs half-cavity with InP and GaAs substrates on respective sides is bowed. This bowing with a radius of curvature of about 1 m occurs because of different values of thermal expansion coefficients of GaAs-based wafers with lattice parameter of 5.6535Å and InP-based wafers with lattice parameter of 5.86875Å, (5.8x10-6 /K for GaAs and 4.8x10-6 /K for InP). After selectively etching the InP substrate the remaining GaAs substrate containing the fused stack re-gains its planarity.

In the second fusion step a second DBR is fused to the InP-based active cavity in the same conditions as during the first fusion. The difference is that the fused stack is not bowed any more. SEM and TEM images (that will be presented elsewhere) shows that the misfit dislocations resulting from the lattice mismatch of GaAs and InP are confined at the fused interface and do not propagate inside the VCSELs structure. Double fused VCSEL wafers are produced systematically without any voids at both fused

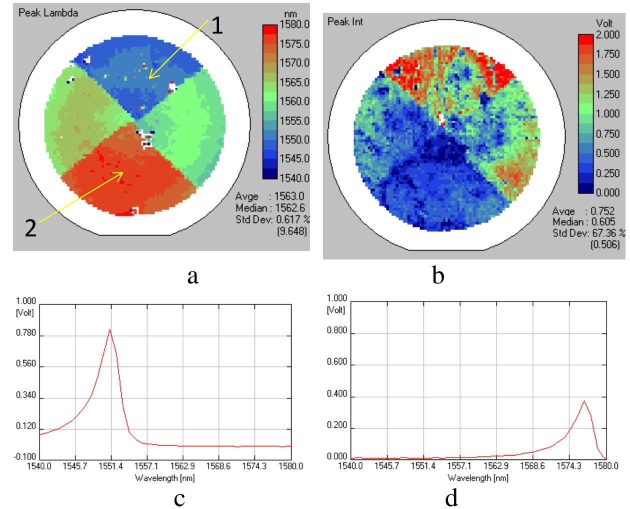


Fig. 3. (a) Peak lambda map, (b) peak intensity map (c) spectrum in point 1 and (d) spectrum in point 2.

interfaces, with a high surface quality over the full 2-inch wafer.One of the big advantage of vertical cavity surface emitting laser technology is the possibility to perform full wafer test without cutting the wafer is parts. In Figure 3 it is presented the pictures of wafer map performed immediately after removing substrate form top DBR side. One can clearly see 4 different wavelength regions, the shortest wavelength is in region denoted by 1 in Figure 3a and the longest is in region denoted by 2. The PL spectra are presented in Figure 3c and d respectively: In Figure 3b it is presented the map of peak intensity. As one can see, the highest intensity it is observed in region 1, the lowest it is observed in region 2. One of the challenges in the future work in developing nano metrology tools for

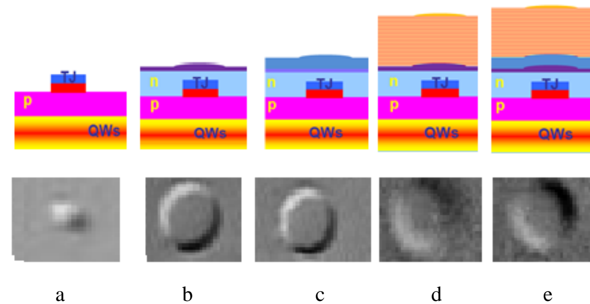


Fig. 4. Images of TJ mesas: a - initially etched 7 µm mesas, b,c- regrown mesas before fusion, d, e - after fusion.

supporting
fabrication technology of longwavelength VCSELs is to find the necessary vertical design and processing flow that will allow correlation between PL map data and device performance.

The processing of the double-fused VCSEL wafer is performed in a standard way. It includes reactive ion etching of the top DBR, selective chemical etching steps in the InAlGaAs/InP active cavity region, dielectric deposition, dry etching steps and e-beam deposition of metals for contacts and electroplating for bond-pads (Figure 5). After wafer qualification by performing on-wafer continuous work (CW) and high frequency (HF) tests, the wafer is thinned and scribed into individual chips. Figure 6 depicts a typical VCSEL chip that is mounted on a sub-mount and electrically

contacted with Au wires by ball-bonding

The 1310 nm range VCSELs fabricated by wafer fusion technique exhibit excellent performance in terms of spectral and power emission in the temperature range up to 100°C as well as modulation response up to 10Gb/s [5,6] .

Fig. 5. Picture of the VCSEL chip with electroplated contact pads

Fig. 6. VCSEL chip mounted on a TO header

The devices from this group showed stable operation with no failures during 5000h, as it is shown in Figure 8. [1].VCSEL mean time to failure (MTTF) value at 25°C and 10 mA bias current was estimated to be in the range of 32 million hours and about 2 million hours at 70 °C [7].

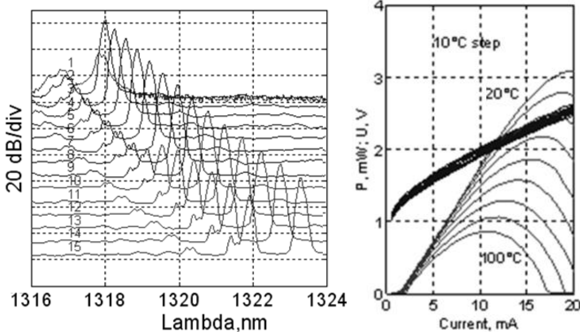


Fig.7. . (a) -Spectral emission at 20°C (the numbers near curves indicate the operation current, curves are shifted down for clarity), (b)- Light-Current-Voltage characteristics up to 100°C

An example of performance versus test time plots, used

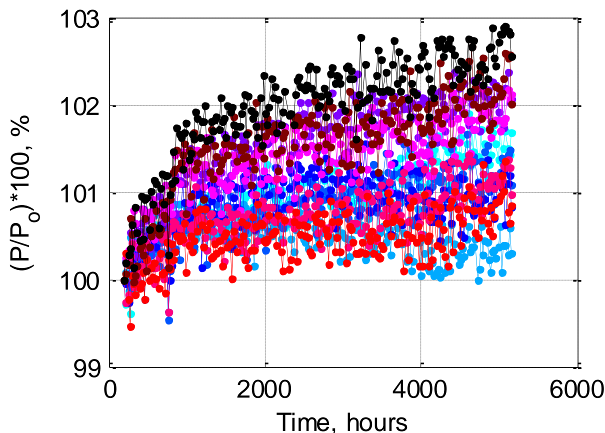


Fig. 8. Power change for 11 devices from qual group showed stable operation with no failures during 5000h

in evaluation MTTF values (as will be presented in [7]) .are depicted in Figure 9-11. The test conditions used for acquisition these plots will be described elsewhere [7].

As one can see from these plots there are more or less steady decreasing of the emission power for all tested devices, and in a few of them the rate of degradation is quite fast (devices under numbers 236, 250 252 and 256).

In this paper we will not try to give a rigorous explanation of the root causes of the device failures, this will be the goal of a long lasting project and will be described in a dedicated publications. The reason to present the experimental results depicted in Figure 8-11 is to describe the initial phase of work in selecting the minimum necessary tools and characterization algorithms for time and cost effective failure analysis.

As one can see from comparison of Figure 8 and Figure 9, under relatively low current and temperature stress there are no devices failures and more than that, there is a small increase in emission power versus test time, while under increased temperature and current stress the threshold current is increasing and emission power is decreasing with time. Without going into more complex analysis, one can conclude that power decrease with time under high temperature and current stress has a component related to increase of threshold current (see Figure 10) as

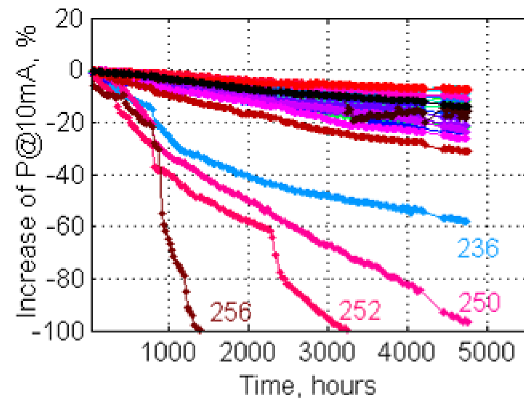


Fig. 9. Plots of changes in power at 10 mA driving current versus time for a set of 24 devices under current and temperature stress

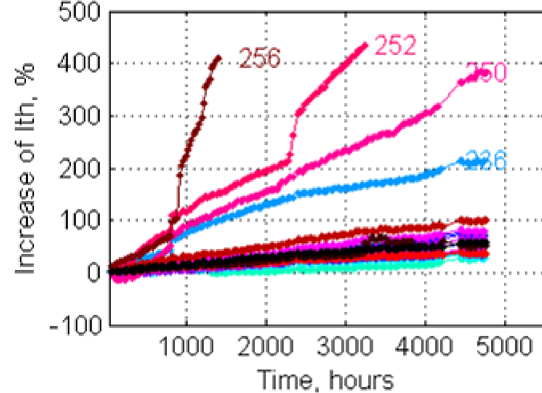


Fig. 10. Plots of changes in threshold current versus time for a set of 24 devices under current and temperature stress

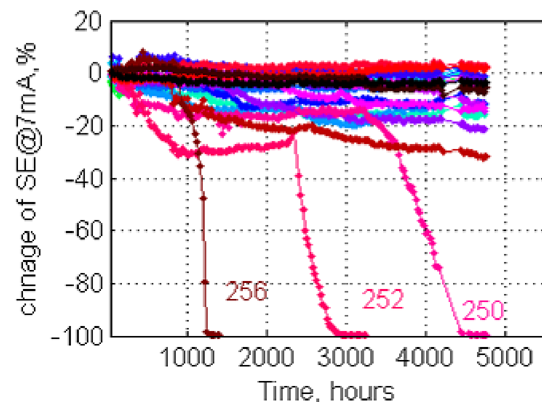


Fig.11. Plots of changes in slope efficiency near threshold current versus time for a set of 24 devices under current and temperature stress

well as related to decrease of slope efficiency (see Figure 11).

IV. ANALYSIS OF THE DEVICE STRUCTURE USING STATE OF THE ART NANO RESOLUTION TOOLS

As one can conclude from the results of the tests of the devices under current and temperature tests, there are device failures during accelerated life tests. Failure analysis is a very challenging, time consuming and costly investigation . One of scientific objectives of the ongoing projects on wafer fused longwavelength VCSELS is to establish the relationship between degradation in VCSEL device performance(e.g., reduction in output power, increase in threshold current, reduction in slope efficiency, electrical short circuits, etc.)

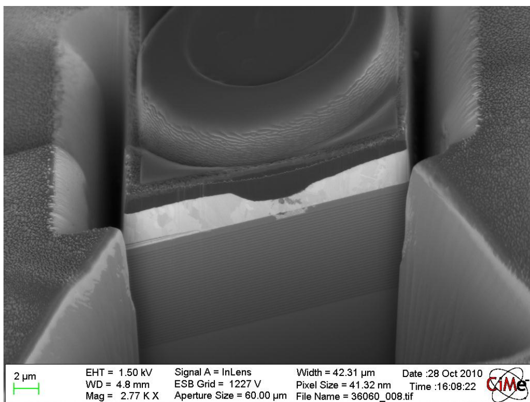


Fig.12. FIB milling around the sample to avoid deposition of the material from milled section

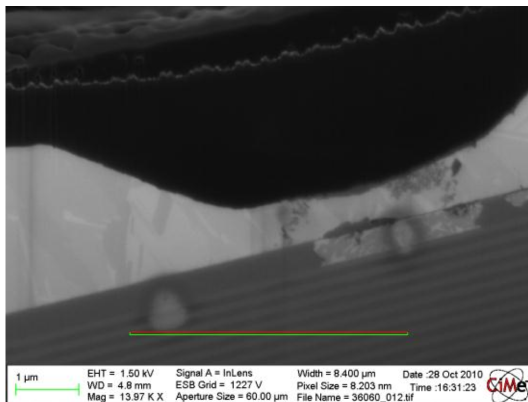


Fig. 13. SEM picture of the identified local diffusion of the gold in InP layer

and devices structure. Understanding this relationship will lead to the identification of specific failure modes and corrective actions for avoiding them, demonstrated using modified fabrication approaches. Achieving this scientific goal will entail the development and perfection of novel analytic tools, such as position-defined transmission electron microscopy (TEM), scanning electron microscopy (SEM) and cathodoluminescence (CL), which will also be useful in a broader area of nano-characterization of complex nano-devices and nano-systems. It should be emphasized that usually such characterization is implemented on micro-structured and nano-structured materials rather than devices, let alone devices fabricated in an industrial environment. The application of such characterization tools is, however, much more difficult and the linkage of the observations to failure modes is extremely complicated for the case of devices (e.g., accurate positioning of the observation area is essential) and needs to be advanced also as a technique by itself.

A feasibility study of the fabrication of focused ion beam (FIB) cross sections was already successfully performed in cooperation with CIME-EPFL. The results of the feasibility study are presented in Figure 12 and Figure 13. A functional VCSEL was wax-mounted on a standard aluminum holder and coated with a very thin gold layer to release the electrostatic charges. The milling around the sample was performed before the tomography was started in order to avoid the deposition of the material from the milled section. This gave an already important result, showing that some of the Au-coating was able to penetrate through the Pt barrier, as evidenced in Figure 14. Device tomography was performed by cutting through the sample every 0.5 um in an automatic mode. In this feasibility study, we were using the automatic mode, but the manual

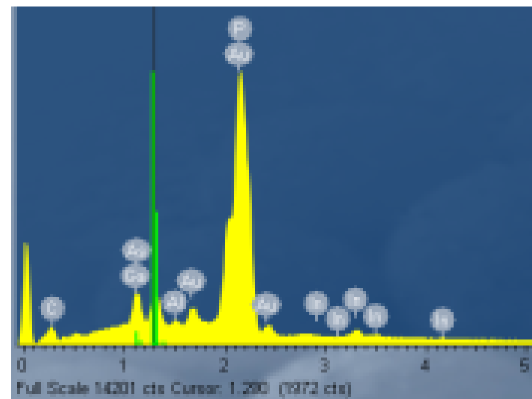


Fig.14. Energy Data Dispersive Scans (EDS) confirming the presence of gold that escaped the Pt barrier

mode in the vicinity of the tunnel-junction allow for getting enough resolution to identify the current confinement aperture , see Figure 16a . In Figure 15 we can notice the appearance of a gap in the structure.The gap could have occurred through the penetration of the etching agents during processing steps. The excess etching time of some layers in the VCSEL structure during processing may have unwanted results such as the GaAs under-etching along fused interfaces. Under-etching of GaAs may cause

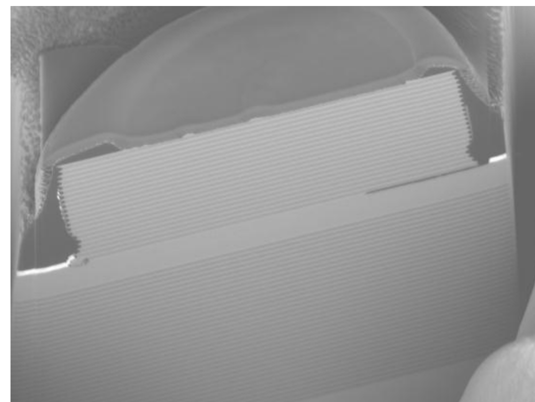
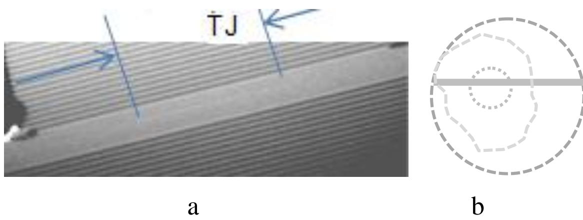


Fig.15. Detailed views of selected elements of the VCSEL structure

the partial delamination of the top DBR from the active structure. Figure 16b depicts the schematic of the top view of the structure, where the dashed line represents the top DBR mesa edge, the irregular shape is constructed from

the successive SEM/FIB images and the full gray line represents the image position depicted in Figure 15. If such a feature will be discovered to be common for wafer fused devices processed in this particular way, this may have a certain impact on VCSEL device reliability.



a b

Fig. 16a-detailed views of selected elements of the VCSEL structure. b-Schematic of the top views of the structure, where the dashed line represents the top DBR mesa edge, the irregular shape is constructed from the successive SEM/FIB images and the full gray line represents the image position depicted in Figure 15 b

A time and cost effective way of detecting hidden features at the fused interface is infrared images taken in sub threshold operation mode, as it is presented in Figure 17. A challenging task is to establish correlations between the contrast observed in infrared near field pictures like presented in Figure 17.Fig. and features observed during FIB tomography (Figure 18). Please note that in this paper the pictures in Figure 15, Figure 17 and Figure 18are not from the same devices.

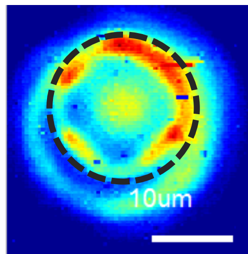


Fig.17. Near field picture of the device under sub threshold current pumping

Another power full tool for characterization of the device structure is cathodoluminescence (CL) [7]. Figure 18. and Figure 19 are presenting the type of images that one can acquire during failure analysis work using CL in long wavelength spectral region.

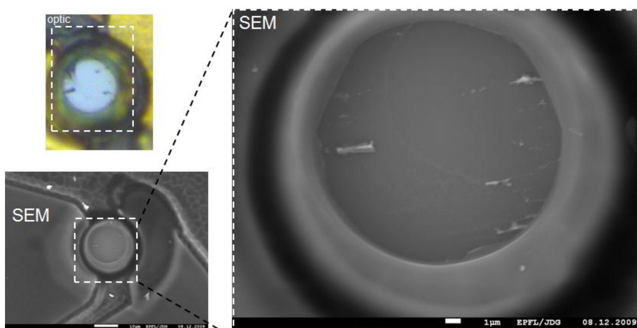


Fig.18. SEM picture of the degraded device after DBR removal. Color inset is the optical microscope picture. There are some residuals after top DBR removal

As one can see, the contrast of the image taken on the same sample in spectral rage of 1220 nm is different form the contrast taken in the range of 1330 nm. Please note the images in Figure 18 and Figure 19 are taken on a device from which top DBR was selectively removed, that is such a failure analysis tool is destructive, as well as cross section image acquisition using FIB.

V. DISCUSSION

As long wavelength VCSELs are emerging as attractive light-sources for replacing DFB lasers for a number of applications, and so far their reliability has always been questioned by the industry as no solid data supporting their reliability was demonstrated, the documented reliability and failure analysis data obtained on wafer-fused VCSELs are of big interest.

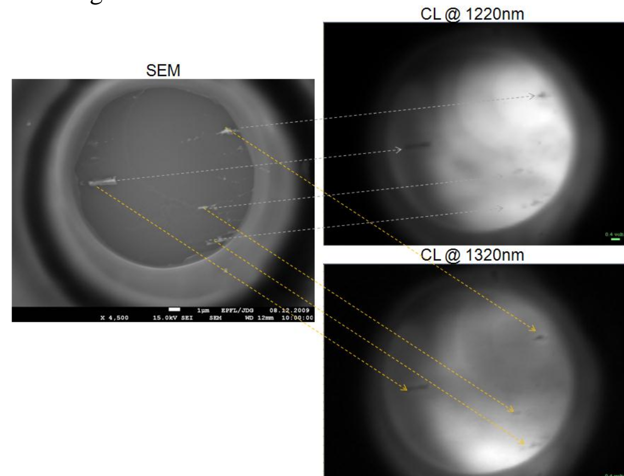


Fig.19. CL pictures (right) at 1220 nm (top) and 1320 nm (bottom).

Results show that VCSELs fabricated with the wafer-fusion technique and displaying high performance level, meet Telcordia generic requirement standards [7], thus making more actual the development of appropriate metrology tools for supporting the fabrication technology and further failure analysis .

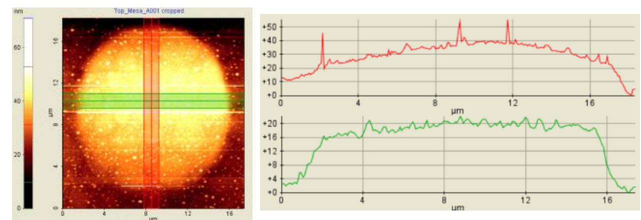


Fig.20. AFM picture at the fabrication step depicted in Figure 4b

Simulations [4] indicates that a very important operation parameter of side mode suppression ratio (SMSR) is sensitive to geometrical dimension of the structured tunnel junction layer. As one can see on Fig. 4 and Figure 20, the vertical and lateral configuration of the epitaxial layer in the vicinity of TJ aperture presents a complex surface with features at nano metric scale. One can demonstrate (it will be presented elsewhere) that a more detailed information on the 3 dimensional shape can be acquired using atomic force microscope(Figure 20) and state of the art optical confocal microscope (Figure 21)

The similar images can be acquired at all processing steps of structuring of the wafer in double fused fabrication process. It is possible even to take pictures of 100 % of the mesas, thus acquiring the necessary information for making statistical correlation between structuring and device performance.

It is very interesting to develop a confocal microscopy tool that will work at wavelengths at which VCSEL materials is transparent. This will allow to detect in the

structures the possible voids as depicted in Figure 15. The work now is in progress to establish correlation between the contrast seen in near field images as depicted in Figure 17 and contrast of the CL pictures (see Figure 19) from one hand, and the voids and trenches that was several times detected by FIB in the double fused VCSEL structures, as in Figure 15. As FIB investigation is destructive , lengthy and costly, a relative simple optical non destructive observation have the potential to become a powerful tool for detection nanometric size defects in a device structure at very early stage of characterization on wafer, thus decreasing the cost of final systems based on VCSELs.

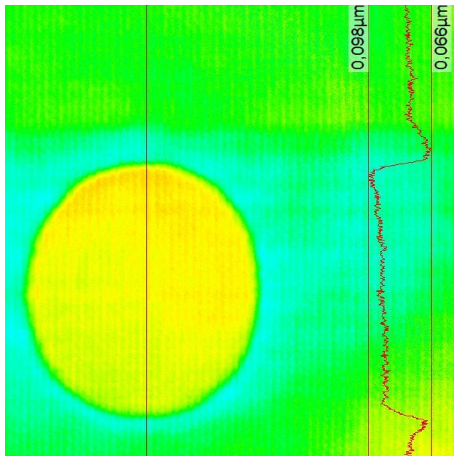


Fig.21. Top view of the surface at the processing step depicted in Figure 4b, taken using confocal optical microscope

Finally, even in the case there will be no structural defects detected in the VCSEL structure by any state of the art nano metrology tools, fabrication of the lamelas (see for TEM CL study presents an ultimate nanocharacterisation tool for revealing the changes in the QWs as a result of accelerated life tests.

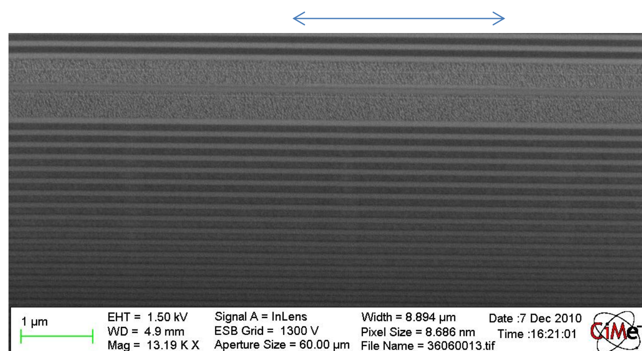


Fig.22. Example of high resolution SEM picture of the TEM lamella fabricated using FIB. Double arrow lined indicated the position of the current aperture defined by buried TJ. CL Figure 22 and TEM study of such a lamella is the subject of ongoing work and it will be presented elsewhere

VI. CONCLUSION

As the work on failure analysis is on its starting stage, the continuous open discussion on implementation of advance nano tools for characterization of the device structure within LPN, BX and international partnership will be crucial for success of this challenging task

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