Journal of Engineering Science *Vol. XXVII, no. 1 (2020), pp. 28 - 35*
Fascicle *Electronics and Computer Science* *ISSN 2587-3474*
Topic *Electronics and Communication* *eISSN 2587-3482*

DOI: 10.5281/zenodo.3713360
CZU 621.3.049.77

3D MICROPACKAGING OF INTEGRATED CIRCUITS

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Received: 01. 15. 2020
Accepted: 03. 05. 2020

Abstract. A major paradigm change, from 2D IC to 3D IC, is occurring in microelectronic industry. Joule heating is serious in 3D IC, and vertical interconnect is the critical element to be developed. Also, reliability concerns will be extremely important: electromigration and stress-migration. This paper presents some actual problems and reliability challenges in 3D IC packaging technology. It shows how different architectures have evolved to meet the specific needs of different markets: Multi Chip Module (MCP); Multipackage module (MPM); Embedded SIP modules; SIP package-on-package (PoP) modules; EMIB (Embedded Multi-die Interconnect Bridge); Silicon-based SIP-Module; 3D-TSV stacked module; SIP variants with combinations of wideband and flip-chip interconnects. Causes of blockages and failure mechanisms, as well as problems with predictive reliability, which will need to be developed in the coming years, are analysed.

Keywords: *prototypage virtuel, Moore's Law, analyse des compromis, reliability.*

Introduction

3D MCM (Multi Chip Module) introduces the IC chip 3D integration technology as well as multilayer interconnected technology of high-density chip, characterized by higher assembly density and capability, more system functions and I/O, lower power consuming and cost, and smaller size [1, 2]. As an important part of electronics devices, the packaging is responsible for the circuit support, protection, I/O connection, heat dissipation and shielding [3]. The new development of electronics devices is placing more new demands on the packages and on the development of packaging materials. The integration of microcircuit packaging trade-off analysis together with functional verification and architectural design results in a complete virtual prototyping solution for the optimization of complex electronic systems [4].

The main driver in today's commercial electronics market is time. Laptops, cell phones and a host of other complex high-density systems often have design cycles of less than a year and even shorter market windows [5]. The very existence of these products depends on finding fast design solutions to meet increasingly demanding performance and cost requirements.

A key to minimizing system cost without compromising time-to-market is to combine manufacturing information with application-specific design information early in the design

process. Including a manufacturing cost analysis in the system design methodology, we can avoid leaving money on the table at the end of development without increasing design time [7]. Common wisdom says that 80% of a product's cost, size and performance (timing, electrical synchronization, power dissipation and reliability) should be spent in the first 20% of the design cycle (Figure 1). Yet this is the part of the cycle for which we have the least mature methods and tools. This part includes requirements capture, specification, trade-off and partitioning. The 80%, which includes some detailed simulation and all physical design, refines and implements the design.

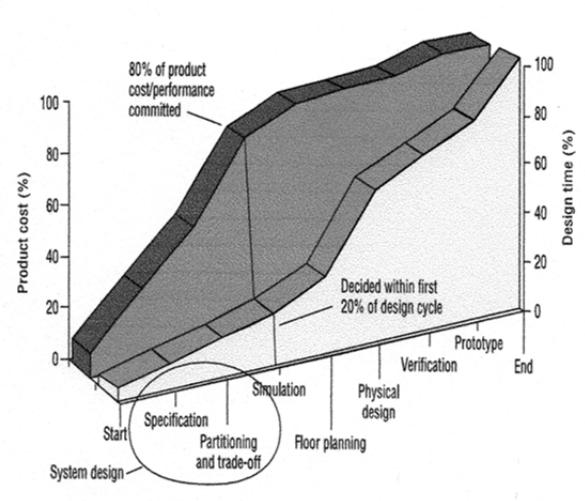


Figure 1. The first cycle of system design should focus on cost, performance, size, power dissipation and system reliability [7].

Moore's Law

In recent years, there has been speculation that Moore's Law is about to come to an end (Figure 2). However, this is not the end of the line. Moore's Law was never just about the number of transistors and nanometres. It was about the benefits of new processes and new models for PCs, data centers, cloud services, embedded products, mobile devices, etc. It was about the benefits of new processes and new models for the future. And the arrival of quantum computing elements, among other things, should give us more ways to achieve further gains [3, 8-10].

The role of trade-off analysis in microcircuit packaging

The future CMOS below 22 nm is delicate and one of the pathways for ultimate system integration is 3D integration requiring the development of via (Through Silicon Via TSV), thinning and substrate assembly technologies to stack chips and substrate levels on top of each other. It also requires the development of new materials for connections (carbon nanotubes, new insulation dielectrics) and new technologies for very low-pitch interconnections. In addition, these processes will have to be "low temperature" to be compatible with most of the structures to be interconnected. Stresses in TSVs, and therefore in the neighboring Si, arise from two sources: *(1)* growth stresses, that arise as a result of via-filling by electroplating, and *(2)* thermo-mechanical stresses that arise due to thermal expansion mismatch between Cu in

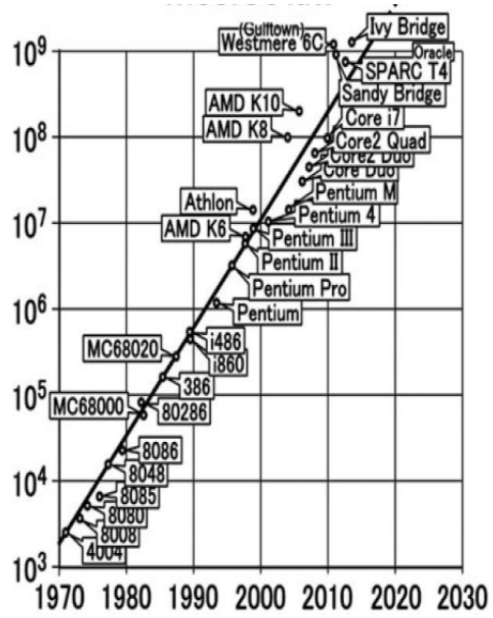


Figure 2. Moore's Law predicts exponential growth of ICs since 1970 (after [3]).

the via and the surrounding Si [11 - 19]. In addition to producing defects (e.g., voids) in TSVs, including complications in electrical performance and potentially causing interfacial and or dielectric fracture, induced stresses also give rise to a plasticity-related phenomenon commonly referred to as Cu pumping, which can have serious reliability implications.

The analysis of the packaging trade-off extends traditional virtual prototyping to include the determination of technology implementation details (Figure 3). The design horizon will depend on your virtual prototype, as you can define exactly how far the virtual prototype extends to describe the system details. Most of the electronics system design community (driven by microcircuit design) defines virtual prototyping as architectural design. Functional verification will provide evidence that the functionality of the system meets the customer's requirements.

The micro/nanopackaging

This is a key point concerning MEMS (Micro Electro-Mechanical System) which requires considering the system as a whole from the point of view of the elementary component, electrical connections, energy sources and storage components, interconnections and mechanical protection. Packaging represents 80% of the cost of the final product and 80% of the causes of failure. MEMS packaging is indeed a complex issue. Moving parts are mechanically very fragile and often require to operate in a relatively high vacuum (< 10^{-2} mbar) in the case of vibrating systems.

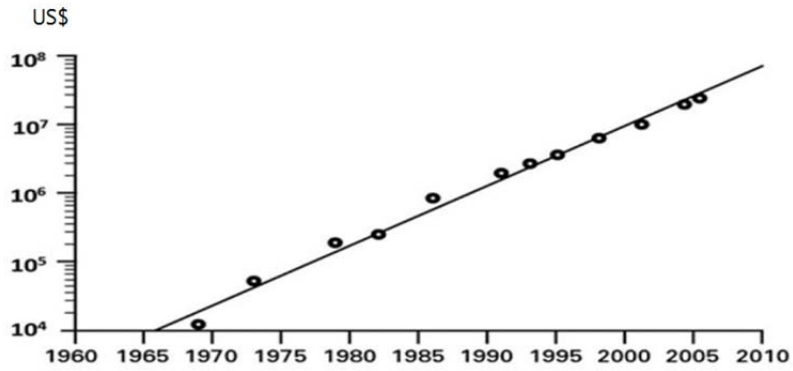


Figure 3. The exponential growth of the cost of lithographic equipment since 1966 [3].

The conventional method for maintaining Moore's Law is to reduce the dimensions of components by lithography - which is increasingly sophisticated and expensive [3]. 3D integration technology - which has been recognized as a technology for realizing future low-cost ICs - provides the third dimension to extend Moore's Law to an ever-higher density, with more functionality and better performance, at lower costs [7].

To realize a small form factor, 3D packaging is required. The market requirements for microelectronics form factor lead to 3D packages that are ultra-light, ultra-thin and with a small footprint. 3D silicon chips are typically 50 ... 100 μm thick and are about 90% thinner than conventional packages. The high-density interconnects in 3D packaging are in the order of 5 ... 20 μm in diameter and more than 90% smaller than those in 2D packaging. Thus, a huge reduction in size and weight could be achieved by replacing conventional packaging with 3D technology (Figure 4) [11]. A small form factor requires a small chip footprint, which is defined as the area of the printed circuit board occupied by the silicon chip.

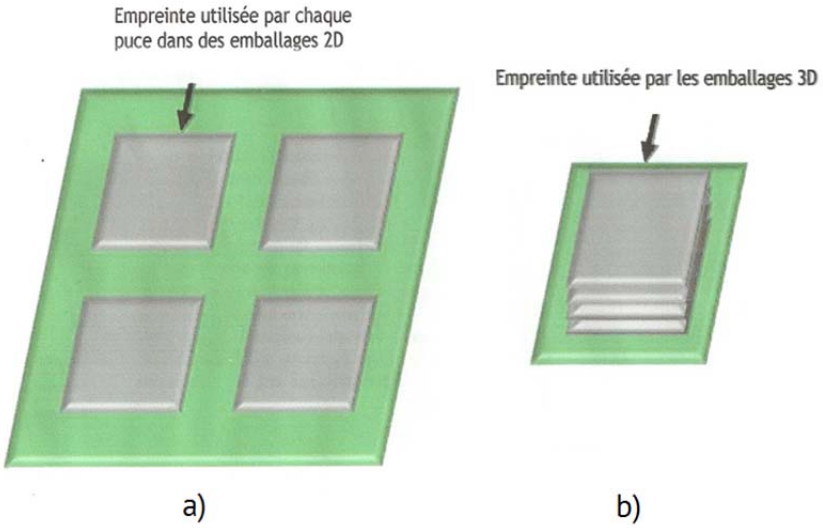


Figure 4. Schematic illustration of the difference footprint between conventional 2D packets (a) and 3D packages (b), (after [11]).

A high-level assembly process flow for a single component is illustrated in Figure 5 to show the typical points in the flow where the wafer, die, and assembled package are tested to check for manufacturing quality or performance.

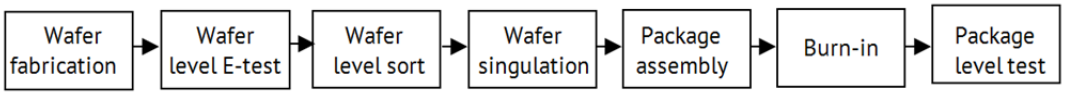


Figure 5. Key steps in a package assembly process.

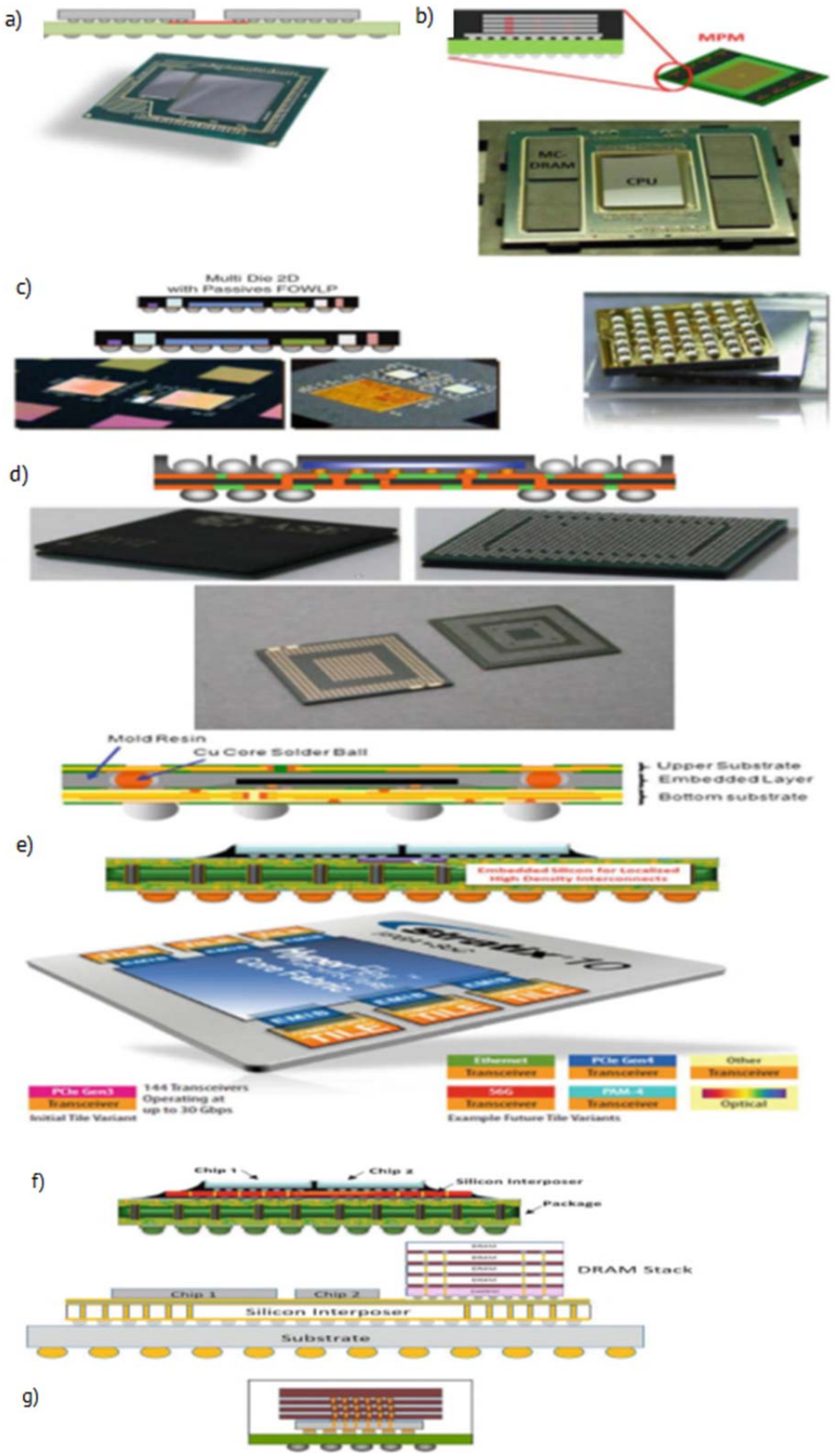
Figure 6 illustrates how different architectures have evolved to meet specific needs for different markets (after [11, 20).

(a) Multi Chip Module (MCP) - Two or more chips are attached in a planar configuration to a packaging substrate (the red line in the schematic drawing indicates that the two or more chips are electrically connected using side interconnects on the package). The image shows the Intel Iris Pro processor with a CPU (the larger of the two chips) and a DRAM chip.

(b) Multipackage module (MPM). One or more chips are packaged before being attached to the final package. The picture above shows the Intel Knight's Landing processor using the MC-DRAM memory module. The MC-DRAM memory module (a memory stack conforming to the Hybrid Memory Cube specification [1]) consists of four stacked memory chips connected by Through Silicon Vias (TSVs), placed on top of a logic chip.

(c) Embedded SIP modules have seamless chip-to-package interconnections and are usually constructed using wafer levels or reconstituted panels [2, 3].

Two packages are stacked on top of each other and connected by peripheral interconnections. Peripheral interconnections can be made using solder balls, Cu rods or solder-coated copper balls. An example of a MCeP (Molded Core embedded Package) is shown in figure 6d. MCeP is the registered trademark of SHINKO electric industries, Co. Ltd. (SIP – a subset of the broader concept of System On Package (SOP) (figure 6e). Its refers to the on-package integration of multiple heterogeneous and/or homogenous ICs, each of which may be in the form of unpackaged die, individually packaged die, or packaged modules.


a)
b)
MPM
MC-DRAM
CPU
c)
Multi Die 2D with Passives FOWLP
d)
Mold Resin
Cu Core Solder Ball
Upper Substrate
Embedded Layer
Bottom substrate
e)
Embedded Silicon for Localised High Density Interconnects
Stratix 10
PCIe Gen3 Transceiver
144 Transceivers Operating at up to 30 Gbps
Initial Tile Variant
Ethernet Transceiver
PCIe Gen4 Transceiver
Other Transceiver
56G Transceiver
PAM-4 Transceiver
Optical
Example Future Tile Variants
f)
Chip 1
Chip 2
Silicon Interposer
Package
DRAM Stack
Chip 1
Chip 2
Silicon Interposer
Substrate
g)

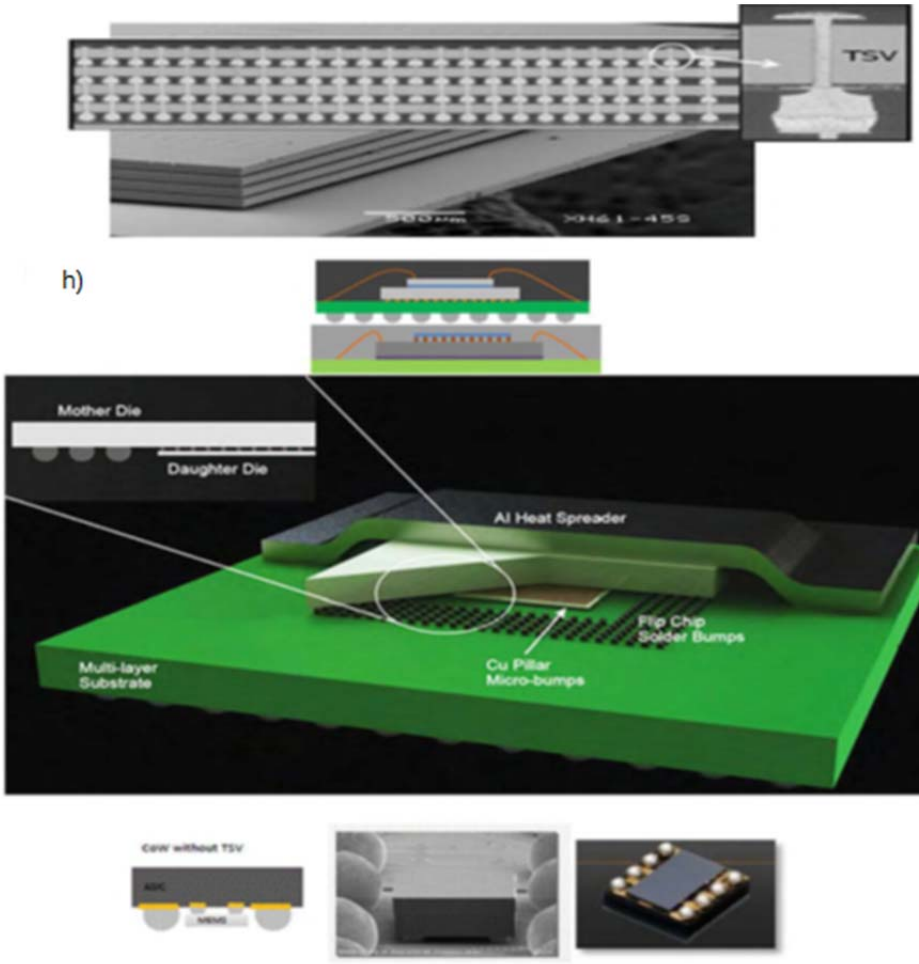


Figure 6. Specific architectures for different markets (after [4, 6, 11, 20):
(a) Multi Chip Module (MCP); (b) Multi Package module (MPM)
(c) Embedded SIP modules; (d) SIP package-on-package (PoP) modules
(e) EMIB (Embedded Multi-die Interconnect Bridge); (f) Silicon-based SIP-Module;
(g) 3D-TSV stacked module; (h) SIP variants with combinations of wideband and flip-chip interconnects.

EMIB-based SIPs use embedded silicon for localized high-density interconnects. The figure 6e shows part of Altera's STRATIX-10 [5]. A silicon interposer is used for thin feature interconnects between different chips or chip stacks (figure 6 f). The interposer has TSVs to connect the chips to the packaging substrate [6]. Multiple chips are stacked using TSV-based interconnects (figure 6g). The figure 6h shows a Micron HMC memory stack. SIP variants include combinations of wideband and flip-chip interconnects. One class of SIP configurations that has driven the most significant technology changes is through silicon vias (TSV)-based SIP [21,22]. The most commonly used interconnect between stacked die for currently available products with TSVs is solder based with interconnect pitches as low as 40 μm (advantage: compliant, also more tolerant to misalignment and lack of coplanarity between bonded surfaces during assembly. However, as the joints become increasingly small, with decreasing interconnect pitches projected below 40 μm for future 3D stacks, the available solder volume will be reduced and a greater proportion of the solder joint will become intermetallic compounds, thus decreasing its compliance [23]. With shrinking interconnect pitch, there is an increasing risk of solder bridging during the assembly process since the joints are closer to each other.

Reliability of micro-nanosystems

A micro-nanosystem can be defined as a system in which at least one functional component is at the micro-nanometric scale [24]. The term "system" implies that one can interact in a controlled manner on its operation. The large initial tensile stress is caused by grain boundary elimination during self-annealing and device fabrication, and is undesirable from the reliability perspective, since this causes large stresses in Si. Because of the potentially serious reliability complications, the role of Cu pumping has been widely studied, and the effects of various process parameters (such as TSV spacing, diameter, Cu overburden after electroplating, and annealing conditions) have been noted [25 - 30]. Although electromigration (EM) is a significant reliability issue in metallic interconnects in electronics, TSVs are generally less susceptible to EM induced failures. Since EM induced interfacial sliding is non-symmetric (and unlike under thermal cycling conditions, it accrues continuously) it may pose a potentially serious reliability challenge, particularly as the current density through the vias increases with decreasing TSV diameter. Stacked packages utilize commercial-off-the-shelf (COTS) packaging which establishes the reliability baseline. The unique reliability issues with package stacking are assembly quality and mechanical shock and vibration effects [31 - 33]. MEMS reliability studies concern the development of knowledge of failure mechanisms and the use of this knowledge to establish predictive models. To date, this is the first brake on the industrialization of MEMS and even more so of NEMS [34 - 35]. The main difficulty comes from the very large diversity of materials and technological processes used (the characteristics of thin films depend on the techniques and conditions of elaboration and these characteristics may change during the device manufacturing process, but also over time or differ from one device to another) [36 - 37]. The lack of recognized techniques for the characterization of MEMS and the lack of standardization in terms of reliability are also important bottlenecks. Predictive reliability is, therefore, still in its infancy and will need to be developed at all costs in the coming years [38].

Conclusion

TSV-based 3D stacking has generated considerable interest, research and development effort in architecture and manufacturing has resulted in a detailed understanding of multiple aspects of the technology. The primary advantages of package stacking are the reduction in substrate area, decreased interconnection lengths and the ability to pre-test packages before stacking. The electrical interconnection length between packages in a stack is less than the length that could be achieved with individual packages arrayed in a planar configuration, decreasing propagation delay. A major advantage of this approach is the ability to pre-test and burn-in devices prior to stacking. Whether at home, in the office or on the move, modern life is increasingly dominated by electronics. For more than 50 years, the development of microelectronic (and now very often nanoelectronic) devices has revolutionized our way of life by offering a vast choice of products and services. Technological progress has made possible the realization of new objects and functions, some of which are giving rise to considerable markets. From safer and more environmentally friendly autonomous cars, to ever more sophisticated fixed and mobile communication systems, to increasingly powerful multimedia and computer equipment, to personal medical assistance systems and leisure activities, the range of applications continues to expand and diversify.

References

1. C. Lee, et al., *Proc. from the 66th Electronic Comp. and Techn. Conf. (ECTC),* Las-Vegas, 31 May-3 June 2016, p. 1439.
2. R. R. Tummala, *Fundamentals of Microsystems Packaging,* McGraw-Hill, New York, 2001, pp. 4-41.
3. D. C. Brock, *Understanding Moore's Law: Four Decades of Innovation,* Chemical Heritage Foundation, Philadelphia, 2006, pp. 67-84.
4. Y. Li, P. K. Muthur Srinath, D. Goyal, *J. Electron. Mater.,* 45(1), 116(2016).
5. L. Li, et al., *Proc. from the 66th Electronic Comp. and Tech. Conf. (ECTC),* Las Vegas, 31 May-3 June 2016, p. 1445
6. T.-M. Băjenescu, "Challenges in Nanotechnologies and Manufacturing Processes," *EEA* vol. 60 (2012), no. 1, pp. 75-79.
7. P. A. Sandborn, and M. Vertal, "Analyzing Packaging Trade-Offs During System Design," *IEEE Design and Test of Computers,* vol. 15, no. 3 (july-sept.), 10-19.
8. T.-M. Băjenescu, "MEMS and their Reliability," *EEA* vol. 58 (2010), no. 4, pp. 7-15
9. Zhiyong Ma and David G. Seiler, "Methodology and Diagnostic Techniques for Nanoelectronics," *Paul Stanford Publishing* 2016, pp. 1089-1119.
10. J. Q. Lu, *Proc. IEEE* 97(1), 18(2009).
11. S. F. Al-sarawi, D. Abott, P. D. Franzon, *IEEE Trans. Comp. Packag. Manufact. Technol.,* 21(1), 2(1998).
12. Yan Li, and Deepack Goyal (Eds.), *3D Microelectronic Packaging,* Springer, 2017.
13. N. Nabiollahi, et al., *Microelectronics Reliability,* 55(5), pp. 765-770, 2015.
14. C.-H. Liu, et al., *Proc. from the 66th Electronic Comp. and Techn. Conf. (ECTC),* Las-Vegas, 26-29 May 2015, p. 1502.
15. C.-H. Liu, et al., *Proc. from the 64th Electronic Comp. and Techn. Conf. (ECTC),* Las-Vegas, 26-29 May 2014, p. 1628.
16. R. Mahajan, et al., *Proc. from the 66th Electronic Comp. and Techn. Conf. (ECTC),* Las-Vegas, 31 May-3 June 2016, p. 558.
17. K. Zoschke, et al., *Proc. from the 60th Electronic Comp. and Techn. Conf. (ECTC),* Las-Vegas, 1-4 June 2010, p. 1385.
18. A. Eitan, K. Hung, *Proc. from the 65th Electronic Comp. and Techn. Conf. (ECTC),* San Diego, 26-29 May 2015, p. 460.
19. T.-M. Băjenescu, "Some Reliability Problems of Electronic Packaging," *Meridian Ingineresc,* no. 4(2014), pp. 22-31.
20. R. Mahajan, and B. Sankman, "3D Packaging Architectures and Assembly Process Design," in Yan Li, and Deepack Goyal (Eds.), *3D Microelectronic Packaging,* Springer, 2017.
21. E. Jan Vardaman, "Foundry and assembly partnerships move the industry forward in tsv technology," http://www.semi.org/en/marketinfo /ctr_041176.
22. Packaging-key for system integration, 27 JUNE 2013, Vila Do Conde, Porto (Portugal).
23. D. P. LaPotin, T. R. Mazzawy, and M. L. White, "Early Package Analysis: Considerations and Case Study," Computer, vol. 26, no. 4, Apr. pp. 30-39.
24. T.-M. Băjenescu, "Reliability Aspects of MEMS and RF microswitches," *Meridian Ingineresc,* no. 4(2015), pp. 13-19.
25. K.-W. Lee, et al., *Proc. from the 64th Electronic Comp. and Techn. Conf. (ECTC),* Orlando, 27-30 May 2014, p. 304.
26. G. Pares, et al., *Proc. from the 11th Electronics Packaging Conf. (EPTC),* Singapore, 9-11 Dec. 2009, p. 772.
27. I. Szendiuch, *Radioengineering,* 20(1), 214(2011).
28. T. M. Bauer, et al., *Proc. from the 59th Electronic Comp. and Techn. Conf. (ECTC),* San Diego, 26-29 May 2009, p. 1165.
29. K. N. Tu, "Reliability challenges in 3d ic packaging technology," *Microelectronic Reliability,* Vol. 51. No. 3, March 2011, PP. 517-523.
30. E. Jan Vardaman, "Foundry and assembly partnerships move the industry forward in tsv technology," http://www.semi.org/en/marketinfo /ctr_041176.
31. Packaging-key for system integration, 27 JUNE 2013, Vila Do Conde, Porto (Portugal).
32. D. P. La Potin, T. R. Mazzawy, and M. L. White, "Early Package Analysis: Considerations and Case Study," Computer, vol. 26, no. 4, Apr. pp. 30-39.
33. T.-M. Băjenescu, "Nano-electronics and Reliability," *EEA* vol. 59 (2011), no. 4, pp. 9-14.
34. T.-M. Băjenescu, "Micro-comutatoare RF MEMS: fiabilitate, moduri și mecanisme de defectare," *Meridian Ingineresc,* no. 3(2013), pp. 11-17.
35. T.-M. Băjenescu, "Some Reliability Problems of Electronic Packaging," *Meridian Ingineresc,* no. 4(2014), pp. 22-31.
36. T.-M. Băjenescu, "Reliability Aspects of MEMS and RF microswitches," *Meridian Ingineresc,* no. 4(2015), pp. 13-19.
37. T.-M. Băjenescu, "Crackings in Microelectronic Packaging," *EEA* vol. 65(2015), no. 2, pp. 15-24.
38. T.-M. Băjenescu, "Zuverlässige Bauelemente für elektronische Schaltungen," *Springer,* 2020.